Abstract—This paper presents a flip-chip packaged 76- to 81-GHz transceiver chip implemented in SiGe BiCMOS technology for both long-range and short-range automotive radar applications. The single chip contains a two-channel transmitter with +18-dBm saturated output power per channel; an LO chain with x4 multiplier, wide-band 20-GHz VCO with -100-dBc/Hz phase noise at 1-MHz offset referenced to a 77-GHz carrier, and divide-by-four prescaler; and a six-channel receiver with 10- to 11-dB noise figure, 14- to 15-dB conversion gain and +1-dBm input P_{1dB} in unpackaged condition. The interconnect loss through the BGA package at 80 GHz is 1.5 to 2 dB. Built-in-self-test (BIST) circuits are integrated to enable RF output power, receiver gain, relative channel-to-channel phase and internal temperature measurement.

Keywords—77 GHz, radar, transceiver, FMCW, receiver, transmitter, SiGe, built-in self test, W band

I. INTRODUCTION

High-performance, low-cost frequency-modulated continuous-wave (FMCW) radar sensors are critical to enable advanced driver-assistance systems in vehicles. These radars must achieve high saturated output power in the transmitter, very low phase noise in the voltage-controlled oscillator (VCO), and high linearity and low noise figure in the receiver [1]. All of these conditions must be met across 25 to 125 °C and the packaging of the radar should have minimal degradation to the overall performance.

Advanced SiGe BiCMOS technology is well suited to meet these radar performance requirements at low cost due to high breakdown voltage in the BJT and high available power gain at W band. Recently, packaged radar chipsets in SiGe have been published which achieve compelling RF performance [2]-[4]; however, most radar chipsets to date have been realized with separate transmitter and receiver chips.

In this paper, we present a single-chip 76-81 GHz transceiver in SiGe BiCMOS with two-channel transmitter and six-channel receiver for both long-range and short-range radar. The chip contains built-in-self-test (BIST) circuits to reduce manufacturing test costs and to support RF functionality. Our transceiver is a second-generation version of the chipset presented in [5], where many individual circuits have been improved, the receiver and transmitter have been co-integrated, a full on-chip BIST infrastructure has been integrated, the RF performance has been improved across the board, and the chip has been co-designed with a ball grid array (BGA) package.

II. TRANSCEIVER DESCRIPTION

A simplified block diagram of the radar transceiver is shown in Fig. 1, consisting of a local oscillator (LO) path, two transmit (Tx) chains, six receive (Rx) chains, and BIST paths. The chip has been implemented in 130-nm SiGe BiCMOS 8HP technology from IBM (now GlobalFoundries) and is designed for robust operation across -40 to +125 °C, V_{CC} from 3.0 to 3.6 V, and process corners.

Local-Oscillator Path: The LO portion of the chip includes a 20-GHz VCO, a frequency doubler to generate a 40-GHz output, and a divide-by-four prescaler to provide 5-GHz outputs to a separate frequency synthesizer. The 40-GHz LO signal is then split and followed by two parallel frequency doublers to generate 80-GHz outputs, one used for the Tx and one for the Rx. To allow use of the transceiver over a frequency range outside of the VCO's range and/or to allow assembly of larger coherent arrays comprising multiple chips, the VCO and first frequency multiplier can be disabled, and an external 40-GHz signal can be directly injected using the “TESTRF” port.

The VCO employs a Colpitts topology and can operate in a wide-band mode for coverage of 77-81 GHz for short-range radar and in a narrow-band mode for coverage of 76-77 GHz for long-range radar. In both modes, phase noise remains extremely low (-112 dBc/Hz at 1-MHz offset from 20-GHz). This is a result of using a transformer-coupled varactor structure [6] which provides high quality factor, low supply pushing, and differential control voltages. Tuning range of the...
VCO is 18.5 to 20.6 GHz, corresponding to radar operation over 74-82.5 GHz, providing additional margin for the system.

Transmitter Paths: Two parallel transmitter chains are included, designed to provide saturated output power at each output of +18 dBm at 25 °C and +16 dBm at 125 °C. The high output power is generated in a two-stage differential power amplifier (PA), each realized as a class-AB balanced cascode structure (schematic found in [5]). The PA has been modified over [5] to achieve both higher and more consistent output power over temperature. An output balun is included to allow for simple connection to external antennas.

The output drivers are preceded by coarse and fine variable-gain amplifiers (VGAs). The coarse VGA is two stages, each consisting of two selectable paths. An inner path provides high gain using a differential cascode structure, whereas an outer path provides low gain using a balanced degenerated cascode structure. This coarse VGA can be used to set the output power to less than -10 dBm. Following the coarse VGA is a fine VGA which can set gain with 6-bit, 0.5-dB resolution. It employs a Gilbert cell with the amount of cross-coupling, and thereby gain, set through a DAC.

Receiver Paths: The receiver includes six parallel channels to enable digital beamforming at baseband for angular detection. Each channel is designed to provide noise figure of 10 dB and input compression point of +1 dBm. The receiver input is first passed through a coupler to allow for injection of an 80-GHz BIST signal and then fed to an LC balun to generate differential RF signals. A mixer-first receiver architecture is used to avoid RF amplification and thereby achieve high linearity. The mixer outputs drive a baseband multiplexer which is used to switch between the down-converted IF signal and baseband loopback test signals. The multiplexer outputs are then buffered and fed off chip. The LO signals are provided to each mixer through a path which includes a three-stage 80-GHz LO buffer, and then a six-way passive power splitter. No transistor-based circuits are used between this splitter and the mixer to avoid any process or temperature-induced variations in phase. As a result, the phase matching between receiver channels remains high.

The receiver mixer is a double-balanced, current-mode structure [2], with schematic found in [5]. A passive transconductance cell, realized as a differential impedance matching network, is used for high linearity. The RF currents are then fed to a switching commutator. The commutator layout has been significantly revised over [5] to reduce LO-to-RF coupling and DC offset. As a result of the reduced coupling, both noise figure and linearity have improved.

Built-in-Test-Paths: The transceiver includes a variety of BIST functions. In the transmitter, power detectors are included at the PA output for measurement of both forward and reflected power (using an on-chip directional coupler) [4]. The forward power detector measurement is used to set the VGA to equalize output power over process, temperature, voltage, and frequency. The reverse power detector measurement is used to monitor impedance mismatch which may be caused by packaging or assembly issues. A power detector is included within the VCO to allow for a digital automatic amplitude control (AAC) loop. Finally, the 80-GHz LO power within the receiver is measured using another power detector.

Fig. 2. Schematic of the RF modulator used for receiver BIST.

BIST for the receiver is more sophisticated. The 80-GHz LO signal is tapped from a directional coupler and used to drive an on-chip single-sideband modulator which consists of quadrature double-balanced 80-GHz mixers, depicted in Fig. 2. The modulator is used to generate FMCW-like signals for injection into each mixer. Baseband inputs for the modulator are sine and cosine signals whose amplitude is controlled through a digital-to-analog converter (DAC) and whose frequency is controlled by an on-chip direct digital frequency synthesizer (DDFS) [3]. The generated IF signal is upconverted by the modulator then the generated phase-modulated RF signal is injected to the Rx mixer [5]. To measure the receiver response, a baseband loopback is included to first measure the modulator input and the receiver's baseband path. Then the modulated input tone power is measured using a power detector located at each mixer input. Finally, the full system is enabled to allow for measurement of the received signal amplitude and phase response at baseband.

III. MEASUREMENTS

The transceiver chip has been implemented in 130-nm SiGe BiCMOS technology. Fig. 3 shows the die photograph of the chip. The die size is 12 mm². For chip-level tests, the die was mounted directly onto a test board, with all signals directly wire-bonded to the board except for high-frequency inputs and outputs which are wafer probed.

Packaging is an essential technology to achieve lower assembly cost for the radar module and a more reliable RF performance. A flip-chip BGA technology is used for the package, with photos shown in Fig. 4. The package size is 9.5 x 8 mm². In designing the package, 3D electromagnetic simulations (HFSS) were used to model the solder-ball and package transitions. Based on this model, the impedance of the receiver and transmitter circuits is compensated to match the impedance of the package interposer and solder mounting transition. Additionally there is an extra matching pattern on the circuit board to adjust the match. To reduce the thermal resistance of the BGA package, the chip has many ground bumps, particularly around the higher-power transmitter circuit.
Packaged-level measurements were conducted by mounting the package onto a test board with transmission lines and probing pads for the mm-wave signals. The pads were probed and the loss of the lines has been de-embedded to move the reference plane back to the package-to-board transition.

Chip-level and package-level measurements are now summarized. The VCO oscillation frequency can be tuned from 18.5 to 20.8 GHz in wideband mode, allowing a transmitter frequency range of 74 to 83.2 GHz. This covers both the 76-77-GHz long-range and the 77-81-GHz short-range radar bands. Supply pushing of the VCO is less than 10 MHz/V at 20-GHz as a result of the power supply rejection provided by the on-chip low-dropout regulator (LDO). Fig. 5 shows the simulated and measured phase noise across frequency and temperature measured at the 5-GHz prescaler output then scaled by 20log(16) to obtain 80-GHz phase noise. Excellent model-to-hardware correlation is achieved. The VCO achieves less than -100-dBc/Hz phase noise at 1-MHz offset at room temperature and -97-dBc/Hz at 125°C, referenced to the 77-GHz carrier. For this result, we use a digital AAC loop to control the VCO’s bias current, helping the circuit maintain high swing at high temperature.

The measured saturated output power of the transmitter is shown in Fig. 6 for both wafer-probed and package measurements. Saturated output power is +15 dBm at the chip output and +16 dBm at the package output. As temperature is increased from 25 to 125 °C, the output power remains high, dropping between 1-2 dB for chip-level and slightly over 2 dB for package-level measurements. If desired, this variation could be reduced to maintain +13 dBm across all conditions through enabling an automatic level control using the on-chip power detector, VGAs, and on-chip ADC.

Turning to the receiver, Fig. 7 shows the measured conversion gain across LO frequency for a 1-MHz IF output for both wafer-probed and packaged measurements. Conversion gain is between 14 and 15 dB on chip, reducing to 12 to 13.3 dB in package. On-chip, the conversion gain reduces by less than 1 dB as temperature is increased to 125 °C. A limitation in our off-chip synthesizer prevented 125 °C measurements of the packaged receiver; thus, we report measurements in package up to 75 °C. From this, we see the same degradation in performance over temperature as with the wafer-probed results. The chip-level gain compression curve versus Vee is shown in Fig. 8. The input P_{1dB} remains above +1 dBm. Finally, the measured chip-level single-sideband noise figure of the receiver at 78.5 GHz is 10.5 dB at 25 °C and 12 dB at 125 °C. The packaged NF at 25 °C is 12 dB.

A small relative phase variation across the receiver channels versus temperature and supply voltage is important for radar system to allow accurate angle measurements. While the phase variation is typically tested and calibrated prior to shipment, the temperature and/or supply voltage sensitivity can degrade the accuracy of this calibration and thus degrade the angular accuracy. As a result, small inherent phase variation is desired. Table 1 shows the phase variation between channels 1 and 4 and channels 5 and 6 across both supply voltage and temperature has been measured using wafer-level probing and the results are summarized in Fig. 9. These results have been normalized...
to the measured phase response at 25°C to illustrate the amount of phase drift which occurs across temperature and supply. The measured phase variation is less than 2° for all conditions.

Each transmit chain consumes 825 mW and each receive chain consumes 103 mW. Total power consumption of the transceiver is 1.8 W in a mode where one transmitter and six receivers are used and 1.6 W in a mode where one transmitter and four receivers are used. A performance summary and comparison to recent radar chipsets is shown in Table I for both chip-level and package-level results.

### Table I. Performance Summary and Comparisons for On-Wafer (Chip) and Package-Level (Pkg.) Measurements

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<tbody>
<tr>
<td>Rx Gain (dB)</td>
<td>2 Chips</td>
<td>2 Chips</td>
<td>1 Chip</td>
<td>2 Pkg.</td>
<td>2 Pkg.</td>
<td>1 Pkg.</td>
</tr>
<tr>
<td>Rx SSB NF (dB)</td>
<td>-10-12</td>
<td>11-12</td>
<td>10.5</td>
<td>-</td>
<td>14-15</td>
<td>12</td>
</tr>
<tr>
<td>Rx ipab (dBm)</td>
<td>&gt; -5</td>
<td>&gt; -2</td>
<td>&gt; +1</td>
<td>-</td>
<td>&gt; -3</td>
<td>&gt; +3</td>
</tr>
<tr>
<td>Rx phase variation (deg)</td>
<td>&lt; 4</td>
<td>+1 to +0.5 *</td>
<td>&lt; 2</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Tx Pout (dBm)</td>
<td>25°C</td>
<td>+16</td>
<td>+17</td>
<td>+18</td>
<td>+14</td>
<td>+11.7</td>
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<tr>
<td></td>
<td>125°C</td>
<td>+14</td>
<td>+15</td>
<td>+16</td>
<td>&gt;12**</td>
<td>+9.6</td>
</tr>
<tr>
<td>Tx Ph. Noise, dBm/Hz</td>
<td>-97.5 to -95</td>
<td>-97 to -100</td>
<td>-99 to -100</td>
<td>-97.5 to -95</td>
<td>-96</td>
<td>-99 to -100</td>
</tr>
<tr>
<td>VCO Range (%)</td>
<td>12%</td>
<td>11%</td>
<td>12%</td>
<td>12%</td>
<td>9%</td>
<td>12%</td>
</tr>
<tr>
<td>Power Consumption (W)</td>
<td>0.79 (4Rx)</td>
<td>1.75 (1Tx)</td>
<td>1.8 (6Rx+1Tx)</td>
<td>0.79 (4Rx)</td>
<td>1.75 (1Tx)</td>
<td>0.85 (4Rx)</td>
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</table>
| * Measured from 25-125°C. ** Estimated from measurements.

### IV. SUMMARY

This paper presents a single-chip packaged transceiver chip for 76- to 81-GHz automotive radar applications implemented in SiGe BiCMOS technology. Each transmitter achieves a saturated output power of +18 dBm at the chip output, while consuming 250 mA from 3.3 V. The VCO achieves a 77-GHz referred phase noise of -100 dBc/Hz at 1-MHz offset across the entire 76-81 GHz frequency band using a single VCO circuit. Each receiver achieves input compression point greater than +1 dBm, noise figure of 10.5 dB, and conversion gain of 15 dB, while consuming 31 mW from 3.3 V. When inserted into a BGA package, Tx output power and Rx noise figure degrade by 1.5 to 2 dB. The transceiver chip consumes 1.8 W in 1-Tx and 6-Rx mode, and 1.6 W in 1-Tx and 4-Rx mode. Compared to the results in [2]-[5], this chip achieves the highest Tx output power, the highest Rx linearity, among the best noise figure, the lowest phase noise, the best power efficiency, and the highest integration level.

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### REFERENCES
