SiGe Technology and Circuits for Automotive Radar Applications

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Abstract—Recent advancements in SiGe device development enable the realization of 77GHz automotive radar systems using relatively low-cost silicon technology. This paper will discuss technology requirements for the radar design and also present examples of receiver and transmitter circuit implementations.

I. INTRODUCTION

Ever since the advent of the seat belt, safety has become a key differentiator in the automotive industry. This trend continued with airbags, anti-lock braking systems, and now with stability control. Although these systems have been pervasive for the past 20 years, the number of accidents and fatalities has basically remained steady in the last 10 years. In 2004, more than 1 million fatalities and 50 million injuries worldwide were related to auto accidents. The economic impact was estimated at 500 billion dollars, equivalent to about 1% of the world’s GDP [1].

In order to make inroads against such staggering statistics, passive systems are no longer sufficient. The next step on the road towards greater safety in automobiles is the use of active sensing to avoid collisions rather than reacting to them. Today, sensor systems based on cameras and radio detection are available in high end automobiles in order to alert and/or provide assistance to the driver in the prevention of a collision.

This paper will cover significant achievements in the development of millimeter-wave SiGe-based technology that have the potential to enable more affordable collision avoidance systems. RF front end circuits such as a novel transmitter with integrated PLL and multichannel receiver at 77GHz will also be reviewed.

II. TECHNOLOGY

Silicon germanium (SiGe) HBT BiCMOS technologies have become the primary technology for mobile handset transceiver applications [2]. More recently, as the SiGe:C HBT device performance exceeded 200GHz $f_T$ and $f_{MAX}$, it becomes feasible to use Si technology for the millimeter-wave markets that had been dominated by III-V compound semiconductors.

One of the critical criteria for successful volume deployment automotive radar system is to base the technology on a low-cost manufacturing semiconductor processing line. A low cost, qualified 0.18μm BiCMOS platform designed for wireless RF transceiver products with a 50GHz $f_T$ and 110GHz $f_{MAX}$ SiGe:C HBT device [3] is used as the baseline technology. In order to achieve the 200GHz $f_T$ and 300GHz $f_{MAX}$ performance targets, the HBT device top structure is modified from a simple quasi-self-aligned structure, with the extrinsic base to emitter dimension set by lithography alignment, to a self-aligned structure with selective SiGe:C base epi integration. Fig. 1 shows the 200GHz xHBT structure, which combines the implanted low resistivity sub-isolation sub isolation buried layer (SIBL) region with a self-aligned, selective-epi base top structure.

Fig. 1. Illustration of the xHBT device.

Aggressive vertical emitter/base profile optimization in conjunction with significant reduction in extrinsic base resistance and utilization of spike anneal for the final emitter anneal allows the SiGe:C device to reach peak $f_T$ of 195GHz and $f_{MAX}$ of 290GHz while maintaining the baseline CMOS device characteristics. Fig. 2 shows optimized device $f_T/f_{MAX}$ performance. This development approach of leveraging the same BiCMOS platform while providing different HBT devices dependent on the target application frequencies reduces risk, shortens technology development time and reduces investment in design kit.

In addition to the SiGe HBT device, the technology also provides passive elements including transmission line, MIM capacitors and thin film resistors. The baseline BiCMOS process provides five layer Cu-metal with thick last metal option.

III. MULTI-CHANNEL RECEIVER

The block diagram of the multi-channel receiver (Rx) chip is shown in Fig. 3. The development of this topology was driven by the need to have a flexible Rx chip in terms of number of channels integrated on a single die,
low power consumption, high channel-to-channel isolation, single-ended or differential IF output usage, and low LO input power level needed. The multi-channel receiver uses an LO signal at half the transmit frequency, typically around 38.25GHz.

Fig. 3. Block diagram of the multi-channel receiver.

Each receiving channel consists of an input LC-balun, a low-noise mixer, and a two stage LO buffer. The balun is an LC-type structure where the inductors are implemented as transmission lines (TL). This enables simultaneous impedance matching and phase and amplitude symmetry.

The double balanced topology developed for the mixer is presented in Fig. 4. Compared to a standard Gilbert cell the RF-pair was split from the LO switching quad (as shown in [4]). This has several advantages. The current in the input RF-pair can be optimized to reduce the input referred noise and to increase the linearity. Thus, the transistors in this pair are biased with the current density needed to get the highest stable gain over temperature (60% of current density for maximum $f_T$). The LO switching quad is biased with much lower current in order to reduce the $1/f$ noise injected by the four transistors (10% of current density for maximum $f_T$). The 2V headroom available at the IF output helps to avoid the clipping in the mixer core.

Fig. 4. Schematic of the modified Gilbert cell mixer (bias network not shown).

An IF buffer is used for differential to single-ended conversion. This buffer consists of two input emitter followers (EFs) and a differential pair extended with EFs at the output (Fig. 3). The first EFs are used for level shift and to buffer the 4mm lines which apply the signal to the differential pairs that are close to the pads. The EFs at the output can drive an external load larger than 500Ω. The differential conversion gain (CG) generated by the mixer is 18dB, enough to de-embed the noise of the IF-buffer. The differential voltage gain of the IF buffer is 6dB. The overall differential gain of one Rx channel is 24dB. This yields a single-ended gain of 18dB at the IF-output. A Rx channel draws 72mA from a 3.3V supply. A photograph of a six channel receiver chip is shown in Fig. 5.

Fig. 5. Photo of a six channel receiver chip.

Each Rx channels’ LO signal is provided by an LO stage consisting of balun, 38.25GHz amplifier, frequency doubler, 76.5GHz PA, balun, and a highly symmetrical, passive LO distribution network (see Fig. 3). The 38.25GHz buffer consists of a cascode stage with inductive load. A differential pair with connected emitters and collectors is the core
of the LO doubler circuit. The antisymmetry (180° phase shift) of the signals taken from the collectors and from the emitters is forced by an AC-coupled λ/2 transmission line at 76.5GHz. The differential signal is then fed into a common-base stage that drives the 76.5GHz PA. This topology has the advantage of equal bias conditions for the devices in the cascode stage, further improving differential operation, stability and signaling. The biasing circuits of all stages are again decoupled from the signal path by λ/4 at 76.5GHz TLs (except for the 38.25GHz path). The 76.5GHz PA consists of a differential cascode. The amplifier, doubler, and PA consume 90mA from a 3.3V supply. The insertion loss of the LO distribution network is 12dB.

A typical single-ended CG of 18dB is measured (this means that on chip the Rx channel generates 24dB). The drop of the gain at 125°C is max 2dB while at -40°C the gain increases by max 1dB. The input referred 1-dB compression point (P1-dB) is -8dBm. The differential CG and P1-dB are 18dB and -2dBm, respectively. This value for the linearity along with this gain represents a record value for 3.3V SiGe receivers. The deviation of the CG between the channels is 0.5dB. The IF noise density at 100kHz is -143dBm(Hz). Using the gain method yields a single-side band NF (NFssb) of 13dB at 27°C at 100kHz which is 4 dB better than the previous reported value for a multi-channel receiver without LNA [5]. At 125°C the NFssb raises up to 15dB only. At 27°C the corner frequency for the noise figure is at 12kHz.

The large signal channel-to-channel isolation is presented in Fig. 6. The Rx channel is driven close to the compression. The isolation in this condition is still better then 55dB. The small-signal S12 between two channels on opposite sides, ch2 and ch5 e.g., is lower then 60dB. The S12 for two adjacent channels is lower than 42dB. This state-of-the-art isolation is achieved placing each Rx channel 1mm apart from the next channel and using a fully differential symmetrical design also for the IF signaling on chip.

Fig. 7 shows the block diagram of the proposed transmitter implemented using an integrated fractional-N frequency synthesizer. The voltage controlled oscillator (VCO) running at 77GHz drives a four stage power amplifier (PA) delivering up to 15dBm [6] [7]. Frequency control is achieved via a PLL including a frequency divider, a phase detector and a loop filter.

Fig. 7. Block diagram of the transmitter with integrated PLL.

The first stage of the frequency divider consists in a dynamic divider by 2 that generates a 38GHz signal used to drive the LO-port of the multi-channel receiver [8]. A static divider achieves then a division by 4. This pre-scaler feeds the programmable divider (PD) whose input frequency is 1/8th the VCO frequency leading to a maximum input frequency of 10GHz. A 3 bit asynchronous divider associated to a 4 bit synchronous counter give a division ratio ranging from 16 to 143. The asynchronous and synchronous blocks use emitter coupled logic (ECL) flip-flop structures made with heterojunction transistor (HBT). Level converters are implemented between CMOS and ECL type circuits: control inputs and at the last divide-by-two output, in order to interface with the digital controller and the phase detector.

The programmable divider is biased by a current source derived from a band gap reference voltage. The current exhibits a positive slope versus temperature allowing current saving when the circuit does not operate at the maximum temperature. At ambient temperature, PD draws typically 75mA from a 3.3V supply. A photograph of the transmitter chip with integrated PLL is shown in Fig. 8.

The phase detector is an XOR gate, made of thin oxide 1.8V CMOS digital cells for maximum speed. It compares the PD output frequency divided by 2 with a 50MHz reference provided by a crystal oscillator. Then a HBT-based level shifter to a 5V supply is used to extend the output voltage dynamic range. As the XOR has a voltage output, the loop filter is a simple RC low-pass filter. In order to have a control voltage range as close as possible to the supply voltage, the XOR must generate extremely
narrow positive or negative pulse. The limit imposed by the XOR bandwidth forces the usable range to be from 0.75 to 4.5V in practice.

A modulator clocked at twice the crystal oscillator reference frequency controls the PD division ratio (Fig. 9). Frequency ramping is generated by a digital integrator controlling the fractional part of the division ratio $\text{frac}$. It is made of an accumulator that adds a 12-bit number setting the Ramp Slope (RS) to the start frequency $F_1$ at each clock cycle, for a ramp up. An overflow detector stops incrementing when stop frequency $F_2$ is reached. In case of ramping down, the accumulator subtracts RS to stop frequency until the underflow detector measures the frequency to be below $F_1$. A 4 wires serial peripheral interface (SPI) allows programming the ramp generator by controlling start, stop frequency and ramping slopes.

Measurements have been performed by using a signal source analyzer E5052B either for frequency or transient domains. To characterize the linear response of the transmitter, a typical triangle transient frequency response was used. Frequencies are computed from measurements made at the PD input. The difference between the measured and expected frequencies indicated an integral non-linearity error of only about 0.3% [9]. Furthermore, the transmitter showed excellent spectral performance with a phase noise equal to -83dBc/Hz at 100kHz offset even at 125°C (see Fig. 10).

Fig. 9. Schematic of the ramp generator and sigma-delta modulator.

V. CONCLUSIONS

This paper presented designs of a transmitter with integrated PLL and multi-channel receiver. The high level of integration and flexibility enabled by such designs, coupled with a low-cost SiGe process technology will certainly aid in the proliferation and implementation of radar sensors in the automotive mass market.

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REFERENCES
