A 16b Quadrature Direct Digital Frequency Synthesizer Using Interpolative Angle Rotation Algorithm

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ABSTRACT
A quadrature direct digital frequency synthesizer (DDFS) is fabricated in 0.35μm CMOS using a new phase-to-sine conversion algorithm. It achieves a spurious-free dynamic range (SFDR) of 96dB with small-sized lookup tables and appropriate arithmetic hardware. The prototype DDFS IC generates 16b cosine and sine outputs with a 0.03Hz frequency tuning resolution at 150MHz sampling rate, consuming 670mW.

INTRODUCTION
A direct digital frequency synthesizer (DDFS) has good characteristics such as agile continuous phase switching, fine frequency resolution, and good spectral purity. However, conventional DDFS implementations have significant area and power disadvantages. First, the conventional approach to synthesis of the digital sine output from the phase information, which is generated by an overflowing phase accumulator, is to use a lookup table [1]. Although some compression methods are applied to reduce the size of the lookup table, its size exponentially increases as the output bit resolution linearly increases. Second, angle rotation algorithms such as a coordinate rotational digital computation (CORDIC) have been used for frequency synthesis [2]. CORDIC can be implemented without the lookup table, but generates higher spurious harmonic tones, compared with the lookup table method. In order to reduce spurious tones, both the internal bit resolution and the number of iterations are increased.

This paper presents a 16b quadrature DDFS using a new phase-to-sine conversion technique named an interpolative angle rotation algorithm. The new algorithm avoids both (a) the large-sized lookup tables needed in the conventional approach and (b) the high internal bit resolution required in CORDIC synthesis.

INTERPOLATIVE ANGLE ROTATION ALGORITHM
The computation of the cosine and sine can be viewed as x- and y-coordinates of the trajectory of unit vector rotation on the unit circle. A rotation can be also divided into several subrotations. Furthermore, the cosine and sine of any angle in [0, 2π] can be evaluated by negation and/or interchange of those of different angle in [0, π/4]. An arbitrary angle θ can be decomposed as θ = mπ/2 + nπ/2^−k + kπ/2^n−k+1 + δ where m is an integer, 0 ≤ n ≤ 2^k−1, 0 ≤ k ≤ 2^l−1, and N and K are fixed design parameters. Then, m, n, k, and δ can be uniquely determined so that 0 ≤ δ < π/2^n−k+1. As shown in Figure 1, the computation of cosine and sine of the angle θ is to rotate by sum of three independent subrotations: fine rotation corresponding to φ = kπ/2^n−k+1 + δ, coarse rotation to φ = mπ/2^l, and final rotation to mπ/2.

The fine rotation is to compute cosφ and sinφ. If cos(kπ/2^n−k+1) and sin(kπ/2^n−k+1) are evaluated in advance and stored in a table, the cosine and sine of kπ/2^n−k+1 + δ can be computed using a polynomial interpolation of those of near angles such as kπ/2^n−k+1 and (k+1)π/2^n−k+1. When a linear interpolation is adopted, cosφ becomes

\[ \cos \left( \frac{k\pi}{2^n} + \delta \right) = \cos \left( \frac{k\pi}{2^n} \right) \cos \delta + \sin \left( \frac{k\pi}{2^n} \right) \sin \delta \]

Also, sinφ can be equivalently obtained. Next, the coarse rotation is to rotate the unit vector by φ. It can be performed by complex multiplication of (cosφ, sinφ) and (cosφ, sinφ), and results in cos(φ+φ) and sin(φ+φ). Finally, the final rotation is to extend the cosine and sine obtained in [0, π/2] into those in [0, 2π], this is accomplished by negation and/or interchange operations. The interpolative angle rotation algorithm only depends on m, n, k, and δ of φ/2^n−k+1 and the output of the phase accumulator is to be already normalized by 2π. Therefore, the additional π- or π/4-multiplication is not needed in the phase-to-sine conversion processing, while most other DDFS methods using either lookup table or CORDIC need it in order to obtain the radian-scaled angle.

IMPLEMENTATION AND MEASUREMENTS
A 32b phase accumulator is used to generate the phase from the input frequency control word. It allows a frequency tuning resolution of f_{fb}/2^{32}, while working in f_{fb}. The 32b adder is partitioned into two 16b carry-select adder sections. Each 16b adder is designed as the Brent-Kung-structured carry-look-ahead adder. As shown in Figure 2, the output of the phase accumulator is truncated to 18b, and fed to each of the rotation blocks.

In the prototype implementation, N and K are set to 3. Then, the most significant 2b are used for the final rotation. The next 3b are used for the coarse table index, and the following next 3b are used for the fine table index. The residual bits are used for the interpolation. Instead of a ROM, the lookup table is implemented with combinational logic, because the size of the table is small. The coarse table consists of only 18b × 7 words of cos(nπ/16) where 1 ≤ n ≤ 7, and each fine table for the cosine and sine also consists of 16b × 8 words for the angles of φ/2^n/128 where 1 ≤ k ≤ 8. In case of the conventional lookup table method, a ROM table of 14b × 2^{12} words is generally needed. Each linear interpolator includes a 15x10 multiplier which is pipelined in 5 stages. The complex multiplier is composed of two adders and four multipliers, and...
each multiplier has 18x17 input word-length and 8 pipelined stages. The internal bit resolution does not exceed 18b. It is only 2b higher than the output bit resolution, while the CORDIC-based one needs the internal bit resolution of 20b to 22b [3]. At the final stage, the 16b cosine and sine outputs are produced by the final rotation, in sign-magnitude, offset binary or 2's complement format.

A prototype DDFS IC was fabricated in 0.35μm 2-poly 4-metal CMOS. It works at a sampling rate of 150MHz. Total power consumption of the entire chip is 670mW with a power supply of 3.0V. The frequency tuning resolution is 0.03Hz. Figure 3 shows the measured waveforms for upper 2b of the final output. Figure 4 shows the measured spectrum of the DDFS output and the SFDR performance for selected output frequencies is plotted in Figure 5; the SFDR is always greater than 96dB. Figure 6 shows a micrograph of the prototype DDFS IC. Die area of the active core is 3.4mm². In Table I, the main characteristics of this work are summarized and compared with other DDFS IC's with output resolutions of 12b to 16b.

CONCLUSION

A prototype DDFS IC fabricated in 0.35μm CMOS uses a new phase-to-sine conversion algorithm which can be constructed with small-sized lookup tables and some arithmetic hardware. It produces 16b cosine and sine outputs with a SFDR greater than 96dB.

REFERENCES


![Figure 1: Basic concept of interpolative angle rotation](image)

![Figure 2: Block diagram of prototype DDFS IC](image)

![Figure 3: Measured waveforms: upper 2b of final cosine output](image)

![Figure 4: Measured digital spectrum](image)

![Figure 5: SFDR performance](image)

![Figure 6: Chip micrograph](image)

<table>
<thead>
<tr>
<th>Chip</th>
<th>Process</th>
<th>Type</th>
<th>Output resolution</th>
<th>SFDR</th>
<th>Max clock rate</th>
<th>Power dissipation</th>
</tr>
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<tbody>
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<td>Quad</td>
<td>16b</td>
<td>100b</td>
<td>100MHz</td>
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<td>66b</td>
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</table>

Table I: Comparison between Different DDFS IC's