Highly Reliable InP-Based HBTs with a Ledge Structure Operating at High Current Density

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SUMMARY

For the InP HBT being developed for 40 Gbit/s optical communication system realization, the effectiveness of the ledge structure for enhancement of device lifetime due to suppressing generation of the surface recombination current is confirmed. An accelerated life test for this structure shows that the activation energy of the mode in which the current gain decreases gradually is 1.7 eV, that the device life extrapolated at 125 °C is more than $1 \times 10^8$ hours, and that this degradation does not depend on the operating current density up to 2 mA/µm². Thus, high reliability at a high current density allowing high-speed design is realized. Also, the degradation mechanism of the current gain is analyzed. It is found that sudden degradation can be controlled by increasing the layer thickness of the emitter and can consequently be eliminated. The above results confirm that the authors’ InP HBT has sufficient reliability for practical implementation. © 2007 Wiley Periodicals, Inc. Electron Comm Jpn Pt 2, 90(4): 1–8, 2007; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/ecjb.20320

Key words: InP HBT; ledge structure; high reliability; high current density.

1. Introduction

InP HBT has both high speed and low power consumption, and its research and development have been in progress with a view to introduction into optical communication systems. Operation of an IC at a level of 100 Gbit/s has been confirmed [1] and applications to OEIC have been studied, because monolithic integration with optical devices is possible [2]. The reliability of such devices, which is an important subject for their practical introduction, has been reported by several organizations. Although there are differences in the device structure and the fabrication method in those reports, an important aspect for obtaining high reliability is suppression of the diffusion of high-concentration p-type dopant and also of surface recombination. The former can be improved by doping carbon with a small diffusion coefficient into the base. With regard to the latter, variation of the current gain can be suppressed by introducing a ledge structure on the external base layer [3–5]. In the authors’ study of the reliability of the InP HBT, the dependence of the emitter mesa orientation on the crystal orientation and a layered structure optimized for deployment of the IC have been shown [6]. In the present research, the effect of our ledge structures with SiN passivation film on reliability is studied. In addition, detailed studies of subjects including the passivation effect and dependence on the operating current density have been performed. In continuous operating tests focusing on the stress conditions of the temperature and the current density, it has been found that the MTTF does not depend on the stress current density from 0 to more than 2 mA/µm². Also, failure analysis suggests the possibility that shifting of the emitter metal is the dominant factor contributing to degradation, providing a guideline for further enhancement of reliability. The above result confirms that the authors’ InP HBT has high reliability meeting practical requirements. Reliability in

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high current density operation is particularly important for applications to high-speed ICs, on which little has been reported.

2. Device Structure and Performance

The HBT used in this research was fabricated by molecular beam epitaxy (MBE) on a 3-inch InP substrate and had an SHBT (single hetero bipolar transistor) structure. The basic structure consisted of an InGaAs collector layer on the InP substrate, a p-type InGaAs base layer doped with high-concentration carbon, and an InP emitter layer doped with Si. An n-type InGaAs was grown on the emitter as an ohmic contact layer. The device fabrication method was almost identical to the case of an epi-layer grown by MOVPE as reported previously [6, 7]. What is significantly different is that dehydrogenation annealing is not needed for MBE-grown wafers. With such annealing, the base resistance is about $570 \, \Omega$. Usually the ledge has a structure formed in order to passivate the external base for protection of its surface. In the authors’ HBT, the shallow remaining parts of the emitter layer, which was fabricated at the formation of the emitter mesa by the non-self-aligning etching technique on the external base region, are used as the ledge. The cross section is shown in Fig. 1. The ledge thickness in the evaluated structure was 20 nm. The ledge width was 70 to 80% of the emitter-to-base spacing. The upper surface of this ledge was eventually covered by an SiN passivation film due to CVD. It was confirmed that the presence or absence of the SiN film affects reliability. The results are presented in the next section. The passivation film for the entire device was BCB (benzocyclobutene). The emitter size of the HBT used in the evaluation was $1 \times 4 \, \mu m^2$. The average performance was a current gain ($\beta$) of 57 and $f_T$ and $f_{max}$ values of 169 and 255 GHz, respectively, at 1 mA/$\mu m^2$. When these values are compared with those for a conventional HBT without ledge ($\beta = 44$, $f_T = 175$ GHz, and $f_{max} = 277$ GHz), it is found that there is an improvement in the DC characteristics while the RF characteristics are little affected.

An accelerated degradation test suffering bias-temperature (BT) stress was performed with the above device. In the test, a DC voltage was continuously applied to about 20 devices within a high-temperature furnace filled with nitrogen. Evaluation of the current and voltage characteristics was performed at room temperature after the current was interrupted.

In the research reported here, two types of HBTs, with emitter InP layer thicknesses of 70 nm (HBT-A) and 20 nm (HBT-B), were used in order to acquire knowledge of the degradation mechanism. In HBT-A, an etch stop layer was inserted, while in HBT-B, the emitter layer was used as the ledge, so that the ledge thickness was 20 nm for both devices.

3. Effects of Ledge and Passivation

Figure 2 shows a comparison of the time variations of $\beta$ with and without the ledge and passivation film. In each, an HBT with a thick emitter layer (HBT-A) was used. The stress condition was $V_{CE} = 2.0 \, V$, the operating current density was $J_c = 1 \, mA/\mu m^2$, and the test temperature $T_a$ was 175 °C. The junction temperature $T_j$ of the device was calculated by using a thermal resistance of $2.98 + 0.008 T_a \, ^\circ C/mW$, which we obtained using another device in the same package separately. Under this condition, $T_j = 213 \, ^\circ C$. It is clear from the figure that the ledge structure is effective in suppressing the initial degradation (within 20 h) of $\beta$. When a SiN film is applied as a protection layer on the ledge, the long-term reliability is also found to be improved.

![Fig. 2. Timewise change of DC current gain with and without a passivation ledge, and with and without SiN passivation film. These plots are for HBTs with a thicker emitter (HBT-A).](image-url)
In the conventional structure without the ledge and SiN, the increase of the base current was found to be significant. This is attributed to the generation of recombination current in the semiconductor surface that has become unstable due to etching. The ledge and the insulation film are found to suppress generation of the recombination current and thus the surface of both the external base and the emitter mesa become stabilized so that reliability is improved.

4. Results of Bias Stress Test: Change in Current Gain

The time variation of $\beta$ during the acceleration test was also studied in detail. All of the test results presented below are for HBTs with both the ledge and the SiN film. Figure 3 compares the time variations of $\beta$ due to differences in the emitter film thickness. Here (a) is for HBT-A and (b) is for HBT-B. The test conditions are identical to those for Fig. 2. In the initial stage after the start of the test, $\beta$ decreases slowly in both devices. However, the long-term variation consists of a continued slow decrease in HBT-A, whereas sudden degradation takes place in HBT-B. In order to distinguish the two degradations in $\beta$ with different characteristics, the gradual decrease appearing initially is called Mode 1, whereas the sudden substantial decrease of $\beta$ is called Mode 2. The Mode 2 failure was observed only in HBT-B under the same stress condition. This suggests that this mode is related to the emitter thickness. By comparison of the time variations of the current–voltage characteristics of HBT-A and HBT-B, the characteristics of the degradations of Mode 1 and Mode 2 are studied. Figure 4 shows the base voltage ($V_{BE}$) dependence of the collector current ($I_C$) and the base current ($I_B$) for typical devices of types HBT-A (a) and HBT-B (b) before the test, during the test, and at failure (HBT-B). In each device, the base current

![Fig. 3. Timewise change of DC current gain for HBT-A and HBT-B under the same stress conditions as in Fig. 2.](image)

![Fig. 4. Typical change in current–voltage characteristics for both $I_C$ and $I_B$ (Gummel plot) (a) for HBT-A and (b) for HBT-B corresponding to Fig. 3.](image)
IB changes over time at a collector current level of $J_c = 1$ mA/µm². In HBT-A, this gradual increase continues to the end (Mode 1) whereas Mode 2 degradation appears in HBT-B so that the base current increases suddenly at 10,016 h. It is seen from Fig. 4(b) that there is a precursor of Mode 2 degradation in the low current density region. Before $\beta$ changes suddenly, an increase of the current component, considered a tunnel current, starts in the low-$V_{BE}$ region. This suggests a recombination-enhanced defect reaction (REDR) [8] similar to the degradation of GaAs HBT. A further discussion of this mechanism will be presented when the TEM image is presented. It is inferred that defect generation brings generation of excessive current and $I_B$ in the high-voltage region increased significantly, so that device failure takes place. Other characteristic changes are variations of the turn-on voltage and increase of the collector leak current. However, both have small changes. Since the turn-on voltage variations are within 20 mV at 10,000 h under accelerated conditions ($T_J = 260^\circ$C), they may be considered insignificant.

In order to study the dependence of the stress intensity on degradation, the current density was further increased. As the current density was increased, the junction temperature also rose. The testing conditions were: testing temperature $T_a$ increased from 160 °C to 195 °C and current density increased from 1 to 5 mA/µm². In order to separate the effect of current stress, a high-temperature storage (HT) test was performed. Figure 5 shows the time variation of $\beta$ when $T_a$ was 195 °C and $J_c$ was 2 mA/µm². (a) shows the results for HBT-A at $T_J = 260^\circ$C while (b) presents the results for HBT-B with $T_J = 230^\circ$C. Also, (c) shows the results of an HT test of HBT-B at 230 °C. From (a), it is confirmed that the degradation speed of Mode 1 increases as the stress is increased and that Mode 2 degradation is generated even if the emitter thickness is large when the junction temperature is high. Comparing Figs. 3(b) and 5(b), it is found that the time at which Mode 2 starts appearing becomes earlier as the stress intensity is increased. In the HT test in (c), $\beta$ decreases gradually but becomes constant after 200 h. Even in the device with a thin emitter, Mode 2 degradation does not appear in the HT test. Hence, Mode 2 degradation is inferred to be caused by the current.

The temperature dependence of device lifetime for each mode is defined as the time over which beta is reduced by 5% and 15% in Mode 1. For Mode 2, the time at which beta suddenly decreases by 15% is defined as each device’s lifetime. Then the median lives for all tested samples were evaluated assuming that they follow the Weibull distribution. Figure 6 shows the junction temperature dependence of the median life for Mode 1. The difference in the stress current density and in the emitter thickness is shown by different symbols. The activation energy derived from the plots is 1.7 eV for a 5% reduction in both types of HBTs.
In the HT tests (0 mA/µm²), most devices do not reach 5% degradation so that only a prediction is given. Since the results for HT tests, in which devices have not suffered electrical stress, are on the line of constant activation energy, Mode 1 failure is dominated by thermal degradation. When the cause of degradation has been inferred, it is considered that the quality of the semiconductor surface, or the interface of semiconductor and SiN film, or the quality of the SiN itself is degraded. Therefore, the main cause is reduction of the surface protection capability.

Figure 7 shows the junction temperature dependence of the median life for Mode 2. The activation energy is estimated to be 1.4 eV. In HBT-A, the number of failures in Mode 2 is low so that predicted values are plotted. From this point the life of Mode 2 of HBT-A can be extrapolated to an even longer life. It is found that the life depends on the emitter thickness for HBT-A degradation.

5. Failure Analysis by TEM of Degraded Devices

For analysis of the causes of degradation, the cross section of the device was observed with a transmission electron microscope (TEM). HBT-A was a device after 1000 h at \( T_a = 195 \degree C \) and 2 mA/µm² with only Mode 1 failure. HBT-B was a device in Mode 2 failure after 200 h under the stress conditions \( T_a = 195 \degree C \) and 5 mA/µm². For comparison, the same part of the sample in HT test was also observed.

With regard to the passivation and ledge, considered to be related to thermal degradation, the state of the semiconductor interface at the ledge did not change much from the state prior to the test. On the other hand, degradation on the semiconductor surface at the external base with the shortest distance between the ledge and the base electrode was observed. In both HBT-A and HBT-B, this situation is seen only for those tested devices. The main cause of Mode 1 is considered to be located here. Next, the variations in the intrinsic region were observed. Figures 8(a) and 8(b) show the cross section from the contact layer and the base layer under the emitter electrode. (a) shows the cross section of HBT-A and (b) the cross section of HBT-B. In both HBT-A and HBT-B, a dark section is seen in the InGaAs contact layer (shown as "1" in the figure). It is characteristic that the dark part progresses inward from the electrode side. Also, this dark section appears to be stopped at the InP layer in Fig. 8(a). When element analysis was performed by energy dispersion X-ray spectroscopy (EDS), Au was confirmed to be present in the dark section. The amount of Ga and As was less than that in the ordinary section. In addition, increases of Ga and As outside the dark section were observed. In addition to this dark section, there was a layer similar to a mutual diffusion layer immediately below the ohmic metal. In such a section, Ti, In, and As were confirmed. In spite of the InGaAs layer, the detected amount of Ga was extremely low. This is because Ti of the emitter metal was diffused toward the semiconductor side by thermal stress. In addition, In and As in the InGaAs layer were diffused to the metal side to form InTix. It has been reported that such a phenomenon occurs in annealing at less than 350 °C and that As is accumulated at the interface between the
metal and the semiconductor [9]. Since the barrier effect of Ti is reduced as InTix is formed, Au is assumed to start diffusing. Since Ga and As were reduced in the dark section observed by TEM, Au was replaced by Ga or As in InGaAs so that AuIn was formed. However, the reported AuIn was shown to occur on annealing at about 350 °C [9]. In the present test, the junction temperature did not reach such a value. Hence, the cross section of the devices is compared with that of the HT test. Figure 8(c) shows the TEM image of the cross section of the device in which there is no change in electrical characteristics after 2000 h at 230 °C for HBT-B. Although there is widespread diffusion of the metal, no dark spot like that in the BT test is observed. Although no analysis by EDS was performed, this phenomenon is assumed to consist of the diffusion of Ti that is often seen in Ti/Pt/Au electrodes in the inward penetration of Au as seen in Figs. 8(a) and 8(b). It is inferred to be attributed to current; that is the electromigration mechanism.

Hence, it is considered that the anomalies generated in the contact layer in (a) and (b) by BT are caused by the same mechanism. However, the situations from the emitter in the lower layer to the base layer are different in HBT-A and HBT-B. In the base layer shown in Fig. 8, there is no anomaly in HBT-A, but there is an anomaly in the crystal structure from the emitter-base junction to the base layer in HBT-B [this is indicated as “2” in (b)]. This is believed to be Mode 2 failure. The anomalous region in this crystal structure is not reflected in the element composition obtained by EDS analysis. Perhaps it is related to some defect. The variations of the IV characteristics suggest a recombination enhanced defect reaction (REDR). A mechanism can be inferred in which some interstitials of Ga, and As, and related defects or their complexes generated in the contact layer move to the InP emitter layer and act as a recombination center. This continuous charge flow results in degradation of the pn junction. Since the frequency of appearance of Mode 2 degradation is related to the InP layer thickness, the life may be determined by the time during which those materials which probably change to recombination centers move through the emitter. In the HT test without generation of such materials, Mode 2 failure does not occur. In a study of the degradation mechanism of lasers, extracted Ga or As was found to become a defect and to act as the recombination center. Further, the defect may become larger or be shifted due to carrier injection, causing sudden degradation [10]. Although the present degradation mechanism is not clear, it is conjectured that a similar mechanism is responsible. Identification of the detailed degradation mechanism and the type of defects will be undertaken.

As discussed above, a mechanism for metal diffusion and sudden degradation triggering the defect generation was inferred. From the test results and the TEM images for devices with different emitter thickness, it was found that a thick InP emitter layer was able to suppress this degradation. Since the InGaAs cap layer thickness is identical in both, the present effect is attributed to the difference in the InP thickness. It is found that the InP emitter thickness is an important parameter in the optimization of highly reliable structures. From the point of view of suppression of the effect of metal diffusion, extending the device life by means of a thicker InGaAs cap layer is equivalent to intro-
ducine refractory metal for the ohmic electrode. We plan to perform studies of the emitter metal for enhanced life. Also, the difference in the metal diffusion suppression capability depending on the cap layer material will be investigated by the introduction of InP.

6. Device Life

As already shown in terms of the junction temperature dependence of the median life, the activation energy of Mode 1 for 5% reduction of the current gain is 1.7 eV and the energy associated with 15% reduction is almost the same. In Mode 2 degradation, the energy is 1.4 eV which was determined from the results of HBT-B because the number of failures is too small to extrapolate the median life in HBT-A. If the same activation energy is assumed in HBT-A, a longer life is expected by extrapolation. This confirmed that the life for Mode 2 depends on the emitter thickness. The life extrapolated to $T_J = 125 \degree C$ (MTTF) is $1 \times 10^7$ h for a 5% reduction of Mode 1 and is more than $1 \times 10^9$ h for a 15% reduction. With regard to Mode 2, a similar life of $1 \times 10^7$ h for a 15% reduction at $T_J = 125 \degree C$ can be obtained with a current density of 2 mA/µm² in the case of an HBT with a thin emitter layer (HBT-B). By increasing the emitter thickness, the life of Mode 2 increases and Mode 1 becomes the dominant factor for life. Hence, at present, a life level of $1 \times 10^9$ h can be guaranteed for a current density of 2 mA/µm² for our HBTs with 70-nm-thick emitter, so that reliability without any practical problems can be confirmed.

7. Conclusions

With regard to the reliability of an InP HBT with ledge, the operating current density dependence and test temperature dependence were studied. Reduction of the DC current gain ($\beta$) was improved from that of the structure without a ledge and the stability of its operation was improved. There are two degradation modes in $\beta$ of the InP HBT. It is probable that the sudden reduction of $\beta$ is caused by emitter electrode migration. It is found that this is not a dominant factor for life if the emitter layer thickness is optimized. In an HBT with a thick emitter structure, which is effective for reliability, the main factor governing the life is thermal degradation around the ledge passivation. Its activation energy is 1.7 eV. Also, the life measured with a 15% reduction of $\beta$ is estimated to be $1 \times 10^9$ h extrapolated to $T_J = 125 \degree C$. It is confirmed that this does not depend on the current density up to 2 mA/µm². This result implies an expansion of the margin of reliability in current density design for high-speed operation of the IC, so that practical applications are guaranteed. From the above results, it is confirmed that the present InP HBT is sufficiently reliable. In the future, further reliability enhancement in the higher current density region is expected by optimization of the semiconductor passivation and introduction of an emitter material with high thermal resistance.

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REFERENCES

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