New Five-Level Active Neutral-Point-Clamped Converter

Eduardo Burguete, Student Member, IEEE, Jesús López, Member, IEEE, and Mikel Zabaleta

Abstract—Multilevel converters are a proven solution for medium-voltage and high-power applications, including renewable energy conversion. Developing 6.6-kV converters is a key goal for the wind turbines industry. Considering the voltage rating of commercially available semiconductors, five-level converters are necessary to reach 6.6 kV. The five-level active neutral-point-clamped converter (5L-ANPC) is one of the most advantageous topologies among five-level multilevel converters. This paper presents a new 5L-ANPC topology that overcomes the features of the previously employed 5L-ANPC topology. Along this paper, the properties and working principle of this new 5L-ANPC are explained. Finally, the validity of the new converter is validated via simulation and experimental results.

Index Terms—AC–DC power converters, five-level active neutral point clamped (5L-ANPC), floating capacitors, multilevel converters, neutral point (NP).

I. INTRODUCTION

MULTILEVEL converters are an attractive solution for medium-voltage and high-power applications, including renewable energy conversion such as wind energy conversion [1]–[4]. They effectively increase the operating voltage of the converter, reducing conduction losses, as well as provide high-quality output waveforms, reduce the size of the output filter, and improve the total harmonic distortion.

The classic multilevel topologies include the neutral point clamped (NPC) [5], the flying capacitor (FC) [6] and the cascaded H-bridge (CHB) [1]–[4]. The three-level NPC (3L-NPC) and the CHB are the most widely employed multilevel converter topologies for industrial applications [1].

In recent years, 3.3-kV three-level classic multilevel converters have been developed and commercialized. Nowadays, the industry is interested in increasing the voltage of the converters to 6.6 kV. With this purpose, and considering the voltage rating of the commercially available semiconductors, five-level converters are necessary.

The classic topologies have serious problems when used to obtain five or more levels. An NPC converter of more than three voltage levels (or a converter with more than one neutral point (NP) [7]) has some problems to balance the voltage of the bus capacitors even for a back-to-back connection. Many modulations and controls have been proposed to solve this issue [8], [9], but it has been proven that there are some operating points where extra hardware [10] or special modulating signals, which distort the output signal, are required to balance the bus capacitors’ voltages [11], [12]. On the other hand, the CHB converter is usually limited to four voltage levels due to the size of the FCs [6]. Finally, the CHB requires isolation to transfer active power [1], [2].

Since the apparition of the classic multilevel topologies, many other topologies have been proposed and studied [1]. Some of them combine the classic topologies, combining the advantages of each one. The most promising five-level topology is the five-level active NPC (5L-ANPC) [13]–[16] shown in Fig. 1. It combines the 3L-NPC and 3L-FC topologies, obtaining advantageous features, such as being able to operate with any modulation index and power factor (PF), solely requiring one FC per phase and providing high-quality output waveforms. However, it connects semiconductors in series and requires additional hardware to control the blocking voltages of the serialized semiconductors.

In this paper, a new 5L-ANPC topology is presented, and its working principle is explained. In Section III, a simple modulation is described to control the introduced topology. Simulation and experimental results in Sections IV and V, respectively, validate the correct operation of the new structure.

Fig. 1. Previously employed 5L-ANPC topology.
II. NEW 5L-ANPC CONVERTER

A. Properties

The new 5L-ANPC converter is presented in Fig. 2. It combines features from the NPC and FC topologies, resulting in two main advantages.

- It only uses one NP like the 3L-NPC, which makes it capable of operating in the four quadrants. An NP voltage balance study for the new 5L-ANPC converter has been carried out as it is done in [17] for the 3L-NPC, obtaining the curve in Fig. 3. At any point below the curve, the NP can be controlled each switching period, and above the curve, a voltage ripple at three times the fundamental frequency appears. In any case, the voltage ripple is controllable at any point using a nearest three vectors (NTV) modulation. This characteristic is independent of the topology and common to multilevel topologies with one NP, that is, it can be observed in the 3L-NPC, in the previously employed 5L-ANPC, and in the proposed 5L-ANPC converter.
- The volume required by the FCs is reduced in comparison with the FC topology, making the construction of the converter feasible. Furthermore, the C1 FC of the new topology is dimensioned like the C1 capacitor of the previously employed 5L-ANPC. C2 and C3 capacitors are much smaller compared with C1, their size is similar to the size of a decoupling capacitor, and no control is required to maintain their voltages at their rated values. Thus, the new 5L-ANPC requires the same number of voltage sensors to control the topology as the previously employed 5L-ANPC ($V_{C1}$, $V_{DC}$, and NP voltage).

The previously employed 5L-ANPC also features these advantages. However, the new 5L-ANPC has two main advantages over the previous 5L-ANPC:

- It does not require any series connection of semiconductors, whereas the previous topology connects semiconductors in series and requires additional hardware to hold their blocking voltage at their rated value. C1, C2, and C3 assure the desired blocking voltage value of all semiconductors in the new topology.
- C2 and C3 capacitors have a snubber-like behavior during commutations that reduces the overvoltage in semiconductors caused by the stray inductance, which is very important in the case of multilevel converters. The stray inductance in multilevel converters may be quite large because the commutation paths are relatively long as they comprise several semiconductors. C2 and C3 shorten the commutation paths in the new topology and, hence, the stray inductance.

B. Operating Principle

The new converter has five voltage levels ($+V_{DC}/2$, $+V_{DC}/4$, $0$, $-V_{DC}/4$, and $-V_{DC}/2$). The operation of the new converter can be divided into two distinct half-periods: the positive and negative half-periods of the output voltage. During the positive output voltage half-period, $C_{BUS1}$ and C1 are used to obtain $0$, $+V_{DC}/4$, and $+V_{DC}/2$ voltages; and during the negative output voltage half-period, $C_{BUS2}$ and C1 are used to obtain $0$, $-V_{DC}/4$, and $-V_{DC}/2$ voltages. Each half-period can be identified with an inner 3L-FC, as shown in Fig. 4. Dotted polygon delimited the inner 3L-FC for the positive half-period, and the dashed polygon delimited the inner 3L-FC for
Similarly to S1 in the previously employed 5L-ANPC, the negative half-period. S7 switches at fundamental frequency during the positive output voltage half-period, hence a (+) is added to 0 in the notation. V9, V10, and V11 are the zero states used during the positive output voltage half-period; hence a (+) is possible to choose between two current paths for the appropriate switching states.

The new topology has 16 switching states available. They are compiled in Table I. V6, V7, and V8 are the 0 switching states; whereas V3, V4, V5, V12, V13, and V14 discharge C1 capacitor.

As aforementioned, selecting appropriate switching states, it is possible to choose between two current paths for +V_{DC}/4 and −V_{DC}/4. For example, Fig. 5 shows the current path with V1, V2, V3, V4, and V5, which are the available switching states for +V_{DC}/4 output voltage. The current flows along the same path for V3, V4, and V5. Thus, there are only two different current paths for +V_{DC}/4 output voltage, which have opposite effect on V_{C1}. V2 charges C1 capacitor; whereas V3, V4, and V5 discharge C1 capacitor.

There are four groups of equivalent switching states (V3, V4, V5), (V6, V7, V8), (V9, V10, V11), and (V12, V13, V14) that affect in the same way the NP voltage and V_{C1}. These switching states can be chosen alternatively. Thus, the available switching states are simplified to eight.

There is only one state possible for +V_{DC}/2 and −V_{DC}/2, and each of them does not have any effect on V_{C1} or on the NP voltage. Zero output voltage affects the NP voltage but does not have any effect on V_{C1}. All +V_{DC}/4 and −V_{DC}/4 switching states charge or discharge C1. V2 and V15 are switching states that do not have an effect on the NP voltage; whereas V3, V4, V5, V12, V13, and V14 are switching states that affect the NP voltage. Table II summarizes the effect on the NP voltage and V_{C1}.

### III. MODULATION OF THE NEW 5L-ANPC CONVERTER

Here, a simple modulation technique is described to control the new 5L-ANPC converter for a three-phase system. The modulation is based on that described in [16], but in our case, the space vector modulation (SVM) technique is used instead of the carrier-based pulselength modulation. A sixth part of the vector diagram for a five-level converter is shown in Fig. 6, where +V_{DC}/2, −V_{DC}/2, and −V_{DC}/4 output voltage levels are denoted by 4, 3, 2, 1, and 0, respectively.

The variables that need to be controlled are the NP voltage and V_{C1} of each phase. V_{C1} of each phase is controlled using redundant switching states (see Table II). Redundant vectors of the SVM are used to control the NP voltage, similarly to the way it is done in the case of the 3L-NPC [17].

The modulation and the control consist of three different stages.

- Based on the reference values of the modulation index (M) and the phase angle (θ), the NTVs are selected.
- A sequence of four vectors (u1, u2, u3, and u4) is selected, where the first (u1) and last (u4) vectors of the sequence are redundant. For example, for the reference voltage vector (V_{REF}) shown in Fig. 6, the sequence may be (421, 420, 320, 310).

The duty cycles (d1, d2, d3) for the (u1, u2, u3) vectors, respectively, are also calculated. Note that u1 vector shares d1 duty cycle with u4 vector. This is determined in the third stage of the modulation.

- Depending on V_{C1} and the phase current, the appropriate switching states for 3 and 1 output voltages are selected in each sequence according to Table II. The switching state that reduces V_{C1} deviation from its rated voltage (V_{DC}/4) is selected.

In the example in Fig. 6, the switching state for 3 and 1 output voltages of 421, 320, and 310 is selected.

- Once the switching states of 3 and 1 output voltages are known, the deviation of the NP voltage produced by the vectors is calculated as

\[
\Delta V_{NP} = \Delta V_{NP}' + \frac{i_{NP,u1} \cdot d_1 \cdot t_{d1}}{f_{mod} \cdot C_{BUS}} + \frac{i_{NP,u2} \cdot d_2}{f_{mod} \cdot C_{BUS}} + \frac{i_{NP,u4} \cdot d_3}{f_{mod} \cdot C_{BUS}} + \frac{i_{NP,u4} \cdot d_1 \cdot (1-t_{d1})}{f_{mod} \cdot C_{BUS}}
\]

where \(\Delta V_{NP}\) is the calculated NP voltage deviation, \(\Delta V_{NP}'\) is the measured NP voltage deviation, \(i_{NP,uj}\) is the current through the NP of \(u_j\), \(d_j\) is the duty cycle of \(u_j\), \(t_{d1}\) is the time distribution of \(u_1\), and \(f_{mod}\) is the modulation frequency.
Fig. 5. Current path for \( i > 0 \). (a) Switching state V2. (b) Switching state V3. (c) Switching state V4. (d) Switching state V5.

TABLE II

<table>
<thead>
<tr>
<th>Switching State</th>
<th>Effect on ( V_{C1} )</th>
<th>Effect on NP voltage</th>
<th>Output Voltage</th>
<th>( V_0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>+V_{DC}/2</td>
</tr>
<tr>
<td>V2</td>
<td>↑</td>
<td>↓</td>
<td>-</td>
<td>+V_{DC}/4</td>
</tr>
<tr>
<td>V3, V4, V5</td>
<td>↓</td>
<td>↑</td>
<td>↑</td>
<td>+V_{DC}/4</td>
</tr>
<tr>
<td>V6, V7, V8</td>
<td>-</td>
<td>-</td>
<td>↓</td>
<td>0(+)</td>
</tr>
<tr>
<td>V9, V10, V11</td>
<td>-</td>
<td>-</td>
<td>↑</td>
<td>0(+)</td>
</tr>
<tr>
<td>V12, V13, V14</td>
<td>↑</td>
<td>↓</td>
<td>↑</td>
<td>-V_{DC}/4</td>
</tr>
<tr>
<td>V15</td>
<td>↓</td>
<td>↑</td>
<td>-</td>
<td>-V_{DC}/4</td>
</tr>
<tr>
<td>V16</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-V_{DC}/2</td>
</tr>
</tbody>
</table>

Fig. 6. Vector diagram for 5L converters (1 sextant).

IV. SIMULATION RESULTS

In order to prove that the new topology works properly, some simulations have been carried out. Some rated values of the simulated converter are shown in Table III.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus voltage, ( V_{BUS} )</td>
<td>10400 V</td>
<td>Minimum time, ( T_M )</td>
<td>30 µs</td>
</tr>
<tr>
<td>Phase current, ( I_{ph, rms} )</td>
<td>850 A</td>
<td>Bus capacitors, ( C_{BUS1} ) and ( C_{BUS2} )</td>
<td>7.8 mF</td>
</tr>
<tr>
<td>Modulation frequency, ( f_{mod} )</td>
<td>2 kHz</td>
<td>Capacitor 1, C1</td>
<td>4.6 mF</td>
</tr>
<tr>
<td>Fundamental frequency, ( f )</td>
<td>50 Hz</td>
<td>Capacitor 2, C2</td>
<td>46 µF</td>
</tr>
<tr>
<td>Dead time, ( T_D )</td>
<td>10 µs</td>
<td>Capacitor 3, C3</td>
<td>46 µF</td>
</tr>
</tbody>
</table>

frequency, and \( C_{BUS} \) is the capacitance of any of the two bus capacitors. In addition, \( t_{d1} \in [0, 1] \).

Setting (1) equal to zero, a simple linear equation arises, where \( t_{d1} \) can be easily calculated and, therefore, the optimal time distribution of the redundant vectors to balance the NP voltage. In case \( t_{d1} > 0 \), then \( t_{d1} = 0 \), and in case \( t_{d1} > 1 \), then \( t_{d1} = 1 \).

Finally, the minimum time, i.e., \( T_M \), is taken into account by adding or subtracting it to the calculated time distribution.

In the example in Fig. 6, the time distribution between 421 and 310 is determined.

A three-phase new 5L-ANPC inverter is considered. The total dc-link voltage \( V_{DC} \) is set to 10 400 V, reaching the desired 6.6-kV line voltage. Each switch supports 2600 V, that is, \( V_{DC}/4 \).
The rated voltage of \( C_{BUS1} \) and \( C_{BUS2} \) is equal to 5200 V. The rated voltages of \( C_1 \), \( C_2 \), and \( C_3 \) are equal to 2600, 5200, and 7800 V, respectively.

The converter is operated under the modulation described in Section III. The second stage of the modulation assures that \( V_{C1} \) is maintained at its rated value, whereas \( C_{BUS1} \) and \( C_{BUS2} \) are kept under control due to the third stage of the modulation that affects the current injection on NP. \( C_2 \) and \( C_3 \) require no control to be maintained at their rated values, as aforementioned.

Modulation frequency \( f_{mod} \) is selected to be 2 kHz. However, the average switching frequency \( f_{sw} \) of any semiconductor of the topology is kept at maximum around 1 kHz, due to the redundancies of the topology [18].

The system has been simulated in many operating points. In this paper, two different operating points are shown. A high modulation index \( M \) is chosen equal to 0.9 (\( M_{max} = 1 \)), and PFs of \( PF = 1 \) and \( PF = 0 \) are chosen to see the different behaviors depending on the PF.

Output voltage and load current of a single phase with \( PF = 1 \) and \( PF = 0 \) are given in Figs. 7 and 8, respectively. The five levels of the converter can be easily identified.

Figs. 9 and 10 show the NP voltage deviation percentages (referenced to the half dc-link voltage, 5200 V) for \( PF = 1 \) and \( PF = 0 \), respectively. With \( PF = 1 \), the voltage ripple is low (below 0.5%), and its frequency is the modulation frequency \( f_{mod} \). With \( PF = 0 \), the voltage ripple is larger (1.5% maximum), and its frequency is three times the fundamental frequency \( f \). This was expectable using Fig. 3, since S1 point (\( PF = 1 \) and \( m = 0.9 \)) is located under the curve and S2 point (\( PF = 0 \) and \( m = 0.9 \)) is located above the curve.

\( V_{C1} \) is controlled every sample time selecting the appropriate switching state for \( +V_{DC}/4 \) or \( -V_{DC}/4 \) output voltages. The maximum \( V_{C1} \) deviation is determined by

\[
\Delta V_{C1,max} = \frac{i_{max}}{f_{mod} \cdot C1}
\]  

(2)

where \( i_{max} \) is the maximum current, \( f_{mod} \) is the modulation frequency, and \( C1 \) is the capacitance.

Figs. 11 and 12 show the \( \Delta V_{C1} \) percentages (referenced to their rated voltage, 2600 V) of the three phases for \( PF = 1 \) and \( PF = 0 \), respectively. The \( \Delta V_{C1} \) percentage is relatively low, around 4.5% at maximum. Furthermore, it can be seen that \( \Delta V_{C1} \) is kept between the boundaries determined by (2).
In addition, C2 and C3 are maintained to their rated voltage without any control, because $V_{C2}$ and $V_{C3}$ deviations depend on the $V_{C1}$ and NP voltage ripples.

V. EXPERIMENTAL RESULTS

A 100-kW prototype was built to test the proposed new topology, which is shown in Fig. 13. It can be seen that the size of C2 and C3 is much smaller than the size of C1. Thus, the size of the new capacitors (C2 and C3) is irrelevant compared with the size of C1.

Hundred-kilowatt rated power was chosen for the prototype to be able to identify any construction problems that may appear when building a high-power converter. However, for the experimental results, much lower power was used ($V_{BUS} = 500$ V and around 10 A).

Fig. 14 shows experimental waveforms of the output voltage (100 V/div) and current (2 A/div) for one phase. The five levels (125 V each) of the converter can be clearly seen.

Fig. 15 shows the experimental voltages (100 V/div) of C1 (125 V), C2 (250 V), and C3 (375 V) and the current (5 A/div) for one phase. As it can be observed, the voltages of all the floating capacitors are kept to their rated value.

Figs. 16–18 show line-to-line voltage (250 V/div), current (2 A/div), and NP voltage deviation (25 V/div) for the operating points E1, E2, and E3 in Fig. 3, respectively. In Fig. 17, the
nine voltage levels of the line-to-line output voltage can be appreciated. In all these three cases, the NP voltage is kept to its rated value. It can be observed that the NP has no voltage ripple in Fig. 16, a relatively large ripple is shown Fig. 17, and a small ripple starts to appear in Fig. 18. This was expected since $E_1$ is located clearly below the limit shown in Fig. 3, $E_2$ is located above the limit, and $E_3$ is located near the theoretical limit.

VI. Conclusion

A new 5L-ANPC topology with some advantageous characteristics over the previously employed 5L-ANPC topology has been presented. Its operating principle has been explained. A simple modulation has been described and applied to the new topology.

Simulation and experimental results have been provided to validate the new topology. The results have shown that the FCs and the NP voltages have been held to their rated values. Thus, the new topology has been proved to work as expected and to be fully controllable.

The new 5L-ANPC topology is an attractive solution to reach the desired 6.6 kV.

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