Integrated Pop-Click Noise Suppression, EMI Reduction, and Short-Circuit Detection for Class-D Audio Amplifiers
Xicheng Jiang, Jungwoo Song, Minsheng Wang, Jianlong Chen, and Sasi Kumar Arunachalam

Abstract—Circuit techniques that overcome practical noise, reliability, and EMI limitations are reported. An auxiliary loop with ramping circuits suppresses pop-and-click noise to 1 mV for an amplifier with 4 V-achievable output voltage. Switching edge rate control enables the system to meet the EN55022 Class-B standard with a 15 dB margin. An enhanced scheme detects short-circuit conditions without relying on overlimit current events.

Index Terms—Audio class-D amplifier, auxiliary driver, auxiliary loop, electromagnetic compatibility, electromagnetic interference, pop-and-click noise, ramping circuit, short-circuit detection, switching edge rate control.

I. INTRODUCTION

CLASS-D audio amplifiers are increasingly used to efficiently drive speakers in mobile communication devices. Mobile devices, such as smartphones and tablets, are typically powered by a lithium battery with a voltage range from 2.5 V to 5.5 V. Power conversion devices between the battery and a Class-D amplifier cause efficiency loss. To maximize the efficiency benefit, a Class-D amplifier must support direct battery connection. Conventional Class-D amplifiers [1]–[3] with a binary pulse width modulation (PWM) produce pulses of 50% duty cycles at zero input signals. This means that external audio-band LC filters are required to reduce quiescent power consumption. These bulky filters are expensive, however, in terms of bill-of-material (BOM) cost and printed-circuit-board (PCB) area. Filter-free Class-D amplifiers [4]–[9], on the other hand, use a ternary PWM to produce very narrow-width pulses with zero input signal. The ternary modulation scheme prevails because of its low quiescent power consumption, even without LC filters. Typical mobile Class-D amplifiers, as shown in Fig. 1, are required to support direct battery hookup, to drive an 8 Ω loudspeaker directly, and to provide more than 1 W output power and better than 90% peak efficiency. State-of-the-art mobile Class-D amplifiers [1]–[10] used a closed-loop architecture, shown in Fig. 2, to reduce distortion and noise and to improve power supply ripple rejection (PSRR). High PSRR at 217 Hz is very critical for a GSM system because RF transmitter bursts at 217 Hz can modulate the battery voltage and cause up to 400 mV of supply disturbance. Although previously reported filter-free Class-D amplifiers [4]–[10] achieved high efficiency and dynamic range, practical concerns for pop-and-click noise (PCN), reliability, and electromagnetic interference (EMI) still limit the full adoption of this technology in mobile devices.
The maximum level of pop-and-click noise is an important audio performance differentiator. During power-up and power-down, the Class-D amplifier produces auditable transients or PCN. Human ears are sensitive to noise in the frequency range from 20 Hz to 20 kHz. The frequency response of human ears is similar to an A-weighted filter. The two major sources of PCN can be identified as the amplifier DC offset and the abrupt start and stop of the PWM pulses during power-up and power-down, as shown in Fig. 3. The DC offset of the amplifier with a certain gain factor is suddenly applied to the amplifier output during power-up and is abruptly taken away during power-down. This abrupt start and stop of PWM pulses causes rail-to-rail transients at the amplifier output. PCN level typically scales with the transient amplitude and the transient duration. The transient caused by the start and stop of PWM pulses is large in amplitude, even though the duration is short. On the other hand, the transient due to DC offset has a long duration, even though the amplitude is small. Both PWM pulse start/stop and DC offset cause harmful pop/click noise, so one of the important design targets was to suppress the transients caused by PWM start/stop and the DC offset of the amplifier simultaneously. To avoid audible PCN, the effective output voltage across a typical 8 Ω speaker during power-up and power-down should be less than ±1.5 mV.

The fast switching time and nearly rail-to-rail signal swing of Class-D amplifiers result in both high efficiency and troublesome electromagnetic interference (EMI). Disturbance from the Class-D amplifier electromagnetic radiation degrades the receiver sensitivity and the performance of other circuits. It is, therefore, mandatory to limit the EMI in mobile devices to meet a generally accepted EN55022 Class-B standard, which is more stringent than the Class-B standard imposed by Federal Communications Commission (FCC). The Class-D amplifier EMI is caused by several factors related to its output waveform, as shown in Fig. 4. Fast switching and rail-to-rail swing cause undesired high-frequency energy. PWM pulses with a fixed switching frequency result in energy concentrated in the modulation frequency and harmonics. The large overshoot/undershoot also produces high-frequency energy. Moreover, large overshoot and undershoot at the driver output stress the output devices and cause concerns about product reliability and lifetime. Class-D amplifier EMI is a design issue, and design for electromagnetic compatibility (EMC) helps shorten the time-to-market.

Integrated Class-D audio amplifiers must be robust and be shut down quickly, and gracefully, to avoid damage when a short-circuit load is connected across the output terminals. A Class-D amplifier typically has an H-bridge switching output stage. To produce output pulses modulated by the input signal, a pair of switches connect one terminal of the speaker to the battery and the other terminal of the speaker to the ground. In case the speaker has a short-circuit, as shown in Fig. 5, the battery is effectively shorted to the ground. The excessive current flowing through the H-bridge circuit not only depletes the battery quickly, but also reduces the IC lifetime due to the excessive electromigration in the metallization and bonding wires. Real-time short-circuit (SC) detection is consequently needed to minimize the time required to detect a short-circuit condition. A typical 8 Ω loudspeaker can have an impedance as low as 4 Ω. The design of accurate SC detection is complicated by the speaker impedance variation and by the continuous switching of the power transistors.

This paper presents circuit techniques that overcome the aforementioned practical concerns and enable the wide adoption of Class-D technology in mobile devices. These include techniques to suppress pop-and-click noise to 1 mV for an amplifier with a 4 V-achievable output voltage level, to reduce EMI and meet the EN55022 Class-B standard with 15 dB margin, and to detect real-time short-circuit conditions without relying on overlimit current events. The paper is organized as follows: The PCN suppression technique is described in Section II. The
EMI reduction technique is presented in Section III. The concept and implementation of real-time short-circuit detection technique are explained in Section IV. The measurement results are presented in Section V. Finally, the conclusions are given in Section VI.

II. POP-AND-CLICK NOISE SUPPRESSION

To illustrate the root cause of PCN from a typical Class-D amplifier shown in Fig. 2, let’s assume that the input signal \( V_{IN} \) of the amplifier is zero and the loop filter output is nonzero due to the DC offset of the loop filter input stage. The comparator inside the PWM generation block (PWM Gen) compares the loop filter output and the reference triangle waveform to produce a PWM pulse. This pulse is applied to the gate of the switching transistor inside the power driver stage, generating the first pulse of the Class-D amplifier after power-up. This first pulse has a magnitude close to the battery voltage and is applied directly to the loudspeaker. Consequently, it produces a very loud pop-and-click. The loop filter provides no help in suppressing this first pulse because there is not yet any feedback from the amplifier output prior to the pulse. This very first pulse is then fed back through the feedback resistor, \( R_{FBNK} \), and subtracted from the input signal \( V_{IN} \). The loop filter integrates the difference and produces the output to counteract this unwanted pulse. Depending upon the unity-gain-bandwidth of the loop filter, it may take many cycles before the initial pulse gets fully suppressed. Finally, the steady-state operation is established with the output average corresponding only to the DC offset of the amplifier, assuming the analog input remains at zero.

To apply PWM pulses to a speaker, a pair of PMOS and NMOS switches, shown in Fig. 6, connects the speaker to the battery and the ground. The effective pulse amplitude across the speaker is given by

\[
V_{eff} = V_{bat} - \frac{R_{spk}}{R_{spk} + R_{SWP} + R_{SWN}}
\]  

(1)

where \( R_{spk} \) is the speaker impedance and \( R_{SWP} \) and \( R_{SWN} \) are the switching on-resistance of transistors \( M_{P} \) and \( M_{S} \), respectively. Equation (1) indicates that the PCN can be reduced by increasing the power switches’ on-resistance \( R_{SWP} \) and/or \( R_{SWN} \). To this end, one approach may be partitioning the output stage into \( N \) stripes, with each stripe having \( N \)-times larger on-resistance. During power-up, only one stripe is turned on and, one-by-one, more branches are turned on until all the stripes are turned on during normal operation. There are two disadvantages associated with this approach. The first is the stability concern about the Class-D loop. When only one stripe is turned on, the switch resistances are \( N \)-times larger than \( R_{SWP} \) and \( R_{SWN} \) and the effective speaker voltage is much smaller than that given in (1). The reduced feedback voltage lowers the overall Class-D loop gain beyond the allowable range for the normal operation mode and adversely affects the stability of the loop. The second disadvantage is that partitioning the output stage to suppress the PCN requires more routing wire and layout area, and incurs more parasitic resistance. In normal operation mode, it is desirable to have the effective \( R_{SWP} \) and \( R_{SWN} \) and the parasitic resistance as small as possible to maximize the power efficiency and output power capability.

The proposed scheme, as shown in Fig. 7, achieves PCN suppression with the least modification of the loop filter design, and leaves the output stage intact. The loop filter and the feedback realized with the resistor \( R_{FB} \) reduce the amplifier distortion and noise and improve the supply ripple rejection. An auxiliary loop formed by a programmable auxiliary driver and resistor \( R_{aux} \) is introduced to suppress the PCN. In addition, the power driver is also designed to have programmable drive strength. Drive strength is ramped up and down during power-up and power-down to produce differential PWM output waveforms, as shown in Fig. 8(a), in contrast to the conventional Class-D output waveform shown in Fig. 3 without pop-and-click suppression circuits. On the other hand, the auxiliary driver is ramped down and up during power-up and power-down to produce differential output \( AUX_{OUT} \), as shown in Fig. 8(b). As a result, the combined feedback strength of the power driver and the auxiliary driver maintains relatively constant during power-up and power-down. At the beginning of power-up, the power driver starts with zero drive strength, which implies \( R_{SWP} \) and/or \( R_{SWN} \) are very large, where \( R_{SWP} \) and \( R_{SWN} \) are the switching on-resistance of the output transistors inside the power driver. At the same time, the auxiliary driver is at full drive strength. The auxiliary path enables the loop to settle without affecting the output voltage across the speaker. During power-up, the strength of the power driver gradually increases until it reaches its maximum, while the strength of the auxiliary driver gradually reduces to zero. This provides a smooth handoff between the auxiliary loop and the main feedback loop. When the loop has settled, the amplifier offset is reflected by the PWM pulse width. As a result, both the PWM pulse amplitude and amplifier offset are ramped simultaneously. The power-down procedure is reversed with respect to the ramping process during power-up. During
Fig. 8. Differential PWM output during power-up and power-down: (a) power driver output and (b) auxiliary driver output.

Fig. 9. Ramping driver strength or driver switching on-resistance.

The normal operation, the AUX driver shuts down, and the main driver fully operates. The AUX driver is much smaller compared to the power driver, since the AUX driver only needs to drive $R_{\text{AUX}}$, which is hundreds of times larger than the typical 8 Ω speaker load. The auxiliary driver, hence the auxiliary feedback loop is active only during power-up and power down. The auxiliary loop is disabled during normal operation.

Fig. 9 illustrates how the power driver switching on-resistance $R_{\text{SWP}}$ is ramped. The switching on-resistance is controlled by the gate voltage of the switching transistor. The switch gate driver has added source impedance, which slows down the transition. For a narrow pulse input to the predriver during power-up and power-down, the output pulse can’t be fully settled within a narrow time window. The output pulse amplitude is limited due to the slow transition. The slow transition time scales with the source impedance. As a result, power driver switching on-resistance, and hence the driver strength, can be scaled by ramping the predriver source degeneration resistance. The detailed implementation of the power driver ramping circuit is shown in Fig. 10, where only half of the H-bridge is shown. The last stage of the predriver has an additional degeneration resistor in series with the ground connection. The degeneration resistors are realized by NMOS transistors $M_1$ and $M_2$. The gate voltage of $M_1$ and $M_2$, $V_{\text{OUTN}}$, is controlled by a slow ramping voltage around the threshold voltage ($V_{\text{TH}}$) of $M_1$ and $M_2$. The low limit of the ramping voltage, $V_{\text{LOW}}$, is slightly below the threshold voltage $V_{\text{TH}}$, while the high limit $V_{\text{HIGH}}$ is higher than the threshold voltage. Instead of using the ground voltage ($V_{\text{SS}}$) and the supply voltage ($V_{\text{DD}}$), $V_{\text{LOW}}$ and $V_{\text{HIGH}}$ are designed to shorten the system power-up time. The NMOS transistor ($M_1/M_2$) does not exit its cut-off region until it is in the subthreshold region when the gate voltage is slightly higher than the threshold voltage. Therefore any ramp-up from $V_{\text{SS}}$ to $V_{\text{LOW}}$ does not help with PCN suppression because the NMOS transistor ($M_1/M_2$) stays in the cut-off region. Similarly, after the NMOS transistor ($M_1/M_2$) has been fully turned on, with the gate voltage reaching $V_{\text{HIGH}}$, further ramp-up does not make much difference. The voltage $V_{\text{OUTN}}$ is thus pulled up directly to $V_{\text{DD}}$ after reaching $V_{\text{HIGH}}$ to further reduce the overall power-up time. The NMOS gate voltage $V_{\text{OUTN}}$ is ramped up by a charge pump circuit, also shown in Fig. 10. The power-up ramp is controlled by clocks $\Phi_1$ and $\Phi_2$, and the power-down ramp is controlled by $\Phi_1$ and $\Phi_3$. During power-up, the $V_{\text{OUTN}}$ is initialized to $V_{\text{LOW}}$, then slowly charged up to $V_{\text{HIGH}}$, and finally pulled up to $V_{\text{DD}}$ for normal operation. The ramping rate depends upon the ratio of the holding cap to the charging cap, which is relatively insensitive to the process-voltage-temperature (PVT) variations. During power-down, the $V_{\text{OUTN}}$ is reset to $V_{\text{HIGH}}$ upon the assertion of the power-down signal, then slowly discharged to $V_{\text{LOW}}$, and finally pulled down to $V_{\text{SS}}$. The auxiliary driver uses the same kind of ramping circuits as described for the power driver. As a result, the ramping rates for the power driver and the auxiliary driver are well matched. The degeneration resistors realized by NMOS transistors for the power driver and the auxiliary driver are also designed with good matching. In addition, the closed-loop Class-D amplifier is designed to tolerate ±3 dB loop gain variation. Consequently, the Class-D loop stability during power-up and power-down are maintained over a wide range of PVT variations.
III. EMI REDUCTION

Mobile devices have to meet radiation standards such as the FCC Class-B standard and the EN55022 Class-B standard before being commercialized. External LC filtering is typically added at the amplifier output pins to improve EMI, but these external filters are the most expensive means of controlling the emission, both in terms of actual filter component cost and the PCB board area. A modulation scheme with constant output common-mode [12] reduces the common-mode induced radiation. But the actual EMI performance achieved depends highly on the PCB layout. The spread-spectrum method [13] cannot provide enough EMI reduction without external filters in the frequency range of concern. A previous report [14] was realized by charging or discharging a 40 pF capacitor connected in feedback around an operational amplifier and the output power transistor. This, however, increases the system complexity and die size. In contrast, a low-cost and robust scheme to slow the edge and hence to reduce EMI at driver output is shown in Fig. 11. The output switching edge rate in this design is controlled by adjusting the transition time of the predriver output. The predrivers in Fig. 11 are realized by inverters, with the addition of source resistors. The slew rate of the predriver output is limited by the RC time constant, where \( R \) is the source resistor value and \( C \) is the capacitor value at the predriver output, which is determined by the gate capacitance of the power transistors. To meet the requirement of large output power capability, large switching output devices (\( M_P \) and \( M_N \) in Fig. 11) are typically used. This means only small source resistors (100 \( \Omega \)–1 k \( \Omega \)) are required to achieve the desired edge rate around 10–20 ns for EMI reduction. The nonoverlapping time is critical to minimize crowbar current. Traditional NOR gate-based circuits are used in this design to generate nonoverlapping time for controlling the gate of driver transistors \( M_P \) and \( M_N \). The nonoverlapping circuits ensure that under no condition are both transistor \( M_P \) and \( M_N \) turned on at any given time. As shown in Fig. 11, source resistors were not only added in the predriver stage, but also in preceding stages. Consequently, the nonoverlapping time was generated to track the slow transition edges. Nonoverlapping time must be larger than the rising/falling time to avoid crowbar current. Because the timing between different stages is determined by the resistors and the gate capacitors of the MOS transistor, the desired timing for controlling transistors \( M_P \) and \( M_N \) can be effectively controlled over process and temperature variations. The slew rate can be easily adjusted by programming the source resistor value. Simulations are performed with three different rising/falling times, which are 0.1 ns, 10 ns and 20 ns. FFT spectrums of the class-D output waveform are computed for frequency up to 400 MHz, as shown in Fig. 12. Simulations indicate the high-frequency peak energy at the amplifier output in the EM band (30 MHz–300 MHz) can be reduced by more than 12 dB with edge rate of 20 ns, compared to a Class-D amplifier without the edge rate control at 0.1 ns rising/falling time, as shown in Fig. 12. Furthermore, edge rate control helps reduce the energy over the entire EM band. Fig. 13 shows that edge rate control smoothes transition edges, reduces the ringing introduced by the bonding wires, and suppresses the overshoot and undershoot, which further reduces EMI and avoids stressing the output driver devices. The reduced overshoot and undershoot makes the design more robust and reliable. On the other hand,
a slow transition time increases the driver dead zone, which is caused by having a minimum achievable pulse width that is greater than zero. The feedback loop in Fig. 7 corrects for the nonlinearity induced by the dead zone. Furthermore, the amplifier efficiency decreases with an increased transition time. Design tradeoffs between efficiency, linearity, and EMI determine the optimal edge rate, which is around 10–20 ns in this design.

IV. SHORT-CIRCUIT DETECTION

Conventional short-circuit detection approaches, shown in Fig. 14, depend on overlimit current events. In Fig. 14(a), the current through the power transistors is measured by sensing resistors in series with the supply and ground lines. When the voltage drop across either resistor exceeds a reference value due to the excessive current flow through the sensor resistor, the short-circuit detection comparator triggers and indicates a “short” signal. The sensing resistors in series with the power switches reduce amplifier efficiency, however, as well as output power capability. Furthermore, the need for accurate sensing resistors makes it unfeasible for integration. In Fig. 14(b), a more feasible overcurrent detection configuration is shown [15]. In this configuration, the current through the power transistors is measured by comparing their drain-to-source voltage to that of two N-times smaller replica transistors that are biased at a reference current. In either case, the short-circuit condition can only be detected when overlimit current events happen. The excessive current can quickly deplete the battery, and the excessive electromigration in the metallization and bonding wires reduces the IC lifetime. Therefore a real-time short-circuit detection scheme that does not rely on over-the-limit current is highly desirable.

The short-circuit detection in this design, shown in Fig. 15, is realized by directly sensing the output pulse when the amplifier input voltage is zero. The small replica of the H-bridge and an on-chip resistor $R_{REF}$ emulate the normal speaker condition and it is used as a reference to compare against short-circuit condition. The signal difference between the normal speaker condition (A) and the short-circuit condition (B) is shown in Fig. 16. Even with zero input, the PWM generation is designed to provide random pulses. The pulse amplitude difference (A–B) between the normal condition and the SC condition exceeds 100 mV when a load less than or equal to 1 Ω is connected across the amplifier output terminals. The amplitude window to detect short is fairly large. So the detection circuits and $R_{REF}$ need not be very accurate. The time window to detect the difference, however, is very narrow. To overcome this issue, a synchronized comparator with a high tracking bandwidth, shown in Fig. 17, is used. The “Derived Clock” signal, CLK, is derived from the current PWM pulse, as shown in Fig. 16. The comparator is strobed on the falling edge of CLK. The comparator reference voltage,
Fig. 17. High tracking bandwidth comparator.

Fig. 18. Die microphotograph.

Fig. 19. Measured Class-D Pop-and-Click level: (a) without PCN suppression circuit and (b) with PCN suppression circuit.

Fig. 20. Measured radiated emission.

Fig. 21. Measured Short-Circuit trigger threshold voltage.

and hence the short-circuit detection threshold voltage, can be easily adjusted. The digital signal processing block in Fig. 15 processes the comparator output signal. The short-circuit detection system does not flag a “short” based on any single short-circuit event. The number of short-circuit events is continuously counted to some preset threshold value within a preset time to flag a short-circuit signal. This makes the proposed short-circuit detection scheme robust and reliable. In case of short-circuit, this design draws about 0.24 A average current from the battery during the 100-μs second window used for detecting short-circuit condition. The detection window is programmable and it can be shorter than the default 100-μs second setting. Once the short circuit is confirmed, the driver can be powered down. So no more current is drawn from the battery. By contrast, the current drawn from the battery in conventional designs can exceed 3 A for large signals before the short-circuit condition being detected. With this scheme, short-circuit conditions are detected before overlimit current events ever happen. It therefore extends battery life and IC lifetime.

V. MEASUREMENT RESULTS

Fabricated in commercial 180 nm CMOS process, the die microphotograph is shown in Fig. 18. The bottom right section is the power driver, with edge rate control for EMI reduction. Pop/click suppression and short-circuit detection are on the top right. The Class-D performance is characterized while the integrated power management units (PMU) is actively operating on the same die.

The amplifier pop-and-click noise level was measured with an Audio Precision analyzer, with A-weighted filtering applied to emphasize the frequency range over which the human ear is sensitive. For a Class-D amplifier with 4 V-achievable output voltage level, the amplifier PCN level was reduced from 27 mV,
Fig. 22. Measured Class-D THD+N versus output power.

Fig. 23. Measured Class-D amplifier efficiency.

shown in Fig. 19(a) with pop-and-click suppression disabled, to 1 mV with the suppression circuit enabled, as shown in Fig. 19(b).

The radiated electromagnetic emission was measured by directly connecting the amplifier to a commercial speaker with an unshielded twisted-pair speaker cable. The device was measured at a 3 m distance, and the standard limit was adjusted accordingly. The Class-D amplifier achieves a 15 dB quasi-peaked margin relative to the EN55022 Class-B standard over a frequency range up to 1 GHz, as illustrated in Fig. 20. It is fair to say that equipment meeting the EN55022 Class-B standard will also meet the FCC Class-B standard.

The short-circuit trigger threshold voltage is measured with zero input signal. The amplifier output load resistance varies from 1 Ω down to 0 Ω. The load resistance at which the short-circuit flag is triggered is recorded for 20 chips. With the default reference voltage setting, the design flags a short-circuit for any load impedance below 0.3 Ω and indicates normal load for any load impedance above 0.7 Ω, as shown in Fig. 21. The spread between 0.3 Ω and 0.7 Ω is caused by the comparator offset.

The measured Class-D THD+N versus output power sweep is shown in Fig. 22. Minimum THD+N is better than −89 dB. Good distortion performance is maintained for up to 1 W of output power. At −40 dB THD+N, the output power reaches 1.02 W with a 4.2 V battery voltage, which corresponds to an output peak voltage of 4.04 V for an 8 Ω load. The Class-D efficiency is plotted against output power in Fig. 23. A peak efficiency of 92% is achieved.

The measured performance is summarized and compared with recent publications in Table I. This amplifier achieves the highest margin to meet the EN55022 Class-B standard and also achieves a low pop-and-click noise level. It is the only reported Class-D amplifier that is capable of detecting a short-circuit condition with zero signal level. And the amplifier also achieves good efficiency and THD+N performance, which implies that circuit techniques overcoming Class-D limitation preserve other advantages of the Class-D technology.
TABLE I
CLASS-D AMPLIFIER PERFORMANCE SUMMARY AND COMPARISON

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<td>-</td>
<td>-</td>
<td>1</td>
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<tr>
<td>Pop-and-click level (mVpk)</td>
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<td>-</td>
<td>-</td>
<td>-</td>
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<td>-</td>
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<td>Short-circuit Detection Scheme</td>
<td>Detection with Zero Signal</td>
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<td>-</td>
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<td>-</td>
<td>Detection Requires Signal</td>
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<tr>
<td>Peak Efficiency</td>
<td>92%</td>
<td>91%</td>
<td>90.9%</td>
<td>93%</td>
<td>79%</td>
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<tr>
<td>Minimum THD+N</td>
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<td>0.028%</td>
<td>0.0012%</td>
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<tr>
<td>Maximum Output Power</td>
<td>1.01W</td>
<td>2.5W with Boost</td>
<td>1.2W</td>
<td>1.6W</td>
<td>0.88W</td>
<td>20W</td>
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<tr>
<td>PSRR @ 217 Hz</td>
<td>89 dB</td>
<td>93 dB</td>
<td>72.2 dB</td>
<td>96 dB</td>
<td>76 dB</td>
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<tr>
<td>Quiescent Current</td>
<td>2.8 mA</td>
<td>2 mA</td>
<td>2 mA</td>
<td>4 mA</td>
<td>3 mA</td>
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VI. CONCLUSION

In conclusion, circuit techniques to overcome practical noise, reliability, and EMI limitations and to enable wide adoption of Class-D technology have been successfully implemented. A pop/click level of 1 mV is achieved, with auxiliary loop and ramp-up/down techniques for an amplifier with a 4 V-achievable output voltage level. A margin of 15 dB beyond the EN55022 Class-B standard is achieved with switching edge rate control. An enhanced scheme detects a short-circuit condition with any signal level, including zero input signals. These practical techniques do not sacrifice amplifier linearity, efficiency, or output power capability.

REFERENCES


Xicheng Jiang received the B.S. degree from University of Science and Technology of China, Hefei, China, in 1991 and the M.S. and Ph.D. degrees in electrical engineering from University of California, Los Angeles, CA, in 1997 and 2002, respectively.

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