A ±0.5% Precision On-Chip Frequency Reference With Programmable Switch Array for Crystal-Less Applications

Yan Lu, Student Member, IEEE, Gang Yuan, Lawrence Der, Wing-Hung Ki, Member, IEEE, and C. Patrick Yue, Senior Member, IEEE

Abstract—An on-chip frequency reference is designed for low-power, low-cost, and fully integrated system-on-chip designs. In this relaxation oscillator, pseudodifferential architecture is used to eliminate frequency variation caused by bias current, and interleave capacitors are implemented to extend its discharge time. A low-leakage programmable switch array (PSA) trimming method is proposed to calibrate the first- and second-order temperature coefficients (TCs) of the composite resistor. The oscillator was fabricated in a 0.16-μm 2P4M CMOS process with an area of 0.162 mm². The oscillator operates at 130 kHz, and measurement results show that it achieves a frequency variation of less than ±0.5% over a temperature range of −20 °C–100 °C and less than ±0.4% over a supply voltage range of 1–3 V.

Index Terms—Crystal-less clock, frequency reference, low-power radio, relaxation oscillator, temperature compensation, wireless sensor networks.

I. INTRODUCTION

A CRYSTAL-LESS receiver is on high demand for low-cost and/or small-form-factor applications, such as AM/FM radios [1] and wireless sensor nodes [2]. The frequency references are usually obtained from quartz crystal oscillators (XOs) that provide stable and low-noise output frequencies or, alternatively, from microelectromechanical system (MEMS)-based oscillators that give comparable temperature coefficients (TCs) and phase-noise performance [3]. However, both XO and MEMS oscillators need additional printed-circuit-board space or system-in-package technology that will increase the volume and the cost. From the energy-efficiency perspective, on-chip solutions should have higher efficiency compared with XO and MEMS oscillators because there is no need to convert between electrical and mechanical energy that would induce extra power loss. Requirements for the frequency reference could be relaxed with novel receiver architectures. For example, in [1], the highly integrated radio receiver with an LC-based voltage-controlled oscillator and a frequency synthesizer can accept a wide range of reference clocks (from 31.13 to 40 kHz with ±100-ppm stability tolerance). A second example allows an even more relaxed frequency variation (±1%) for communication links such as the universal asynchronous receiver/transmitter [4]. It means that the absolute value of the reference clock is not as important as its immunity to temperature and supply voltage variations. Thus, accuracy could be traded off for better stability for on-chip frequency reference designs. Relaxation oscillators are good candidates for low-power operation with tolerable accuracy [5]. The frequency spread within ±0.5% after two-point trim is achieved in [2], consuming a current of 42.6 μA, and frequency variations of ±0.68% and ±0.82% with respect to temperature and supply voltage, respectively, are accomplished with only 280 nW in [4]. Moreover, a relaxation oscillator has the advantages of large tuning range and small area [6].

Table I summarized and compared the general performance of different types of reference generators. The MEMS oscillator is not power efficient as it consumes over 5 mA for submegahertz-range oscillation frequencies [3]. A TC-compensated on-chip LC oscillator could achieve an accuracy better than ±100 ppm; however, it still dissipates large power since its core oscillation frequency is usually in the gigahertz range [7]. On the other hand, a relaxation oscillator consumes the lowest power with relatively low oscillation frequency and acceptable frequency stability, indicating that it could be the best choice for ultralow-power, low-cost, and compact-size communication applications.

The frequency drift of a relaxation oscillator is mainly caused by the variations of polyresistors and bias currents due to process, voltage, and temperature. On-chip resistors have relatively large TCs compared with capacitors; hence, a composite resistor with two types of resistors (positive- and negative-TC resistors) is commonly employed to achieve a zero/low-TC resistor [4]. However, process variations of those two resistors

![Table I: Comparison of Different Types of Oscillators](image)

<table>
<thead>
<tr>
<th>Oscillator</th>
<th>Crystal</th>
<th>MEMS</th>
<th>LC</th>
<th>Relaxation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Location</td>
<td>On-board</td>
<td>In-package</td>
<td>On-chip</td>
<td>On-chip</td>
</tr>
<tr>
<td>Frequency</td>
<td>1 kHz - 100 MHz</td>
<td>200 kHz - 200 MHz</td>
<td>~GHz</td>
<td>1 kHz - 10 MHz</td>
</tr>
<tr>
<td>F variation</td>
<td>±1-100 ppm</td>
<td>±10 ppm</td>
<td>±100 ppm</td>
<td>±10 ppm</td>
</tr>
<tr>
<td>Current (Iq)</td>
<td>100 nA - 50 mA</td>
<td>5 mA - 50 mA</td>
<td>~10 mA</td>
<td>10 nA - 100 μA</td>
</tr>
<tr>
<td>Iq/F</td>
<td>Med. @ kHz</td>
<td>High @ MHz</td>
<td>High @ kHz</td>
<td>Med. @ MHz</td>
</tr>
<tr>
<td>Cost</td>
<td>Medium</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
</tr>
</tbody>
</table>

Manuscript received March 13, 2013; revised May 23, 2013; accepted July 14, 2013. Date of publication August 22, 2013; date of current version October 14, 2013. This brief was recommended by Associate Editor S. Levantino.

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Digital Object Identifier 10.1109/TCSII.2013.2277984
are uncorrelated and could go in opposite directions and result in TC that is worse than predicted [8], [9]. Moreover, post-fabrication trimming of either the positive- or the negative-TC resistor array requires large switches that introduce error due to leakage current.

In this brief, pseudodifferential architecture is employed to improve frequency variation caused by bias current, and a novel programmable switch array (PSA) trimming method is proposed to achieve low-TC frequency reference in Section II. Measurement results are given in Section III, followed by discussions and conclusions in Section IV.

II. CIRCUIT IMPLEMENTATION

A. Conventional Relaxation Oscillator

A conventional relaxation oscillator is realized by monitoring the voltage of the capacitor that is charged by $I_C$ and discharged by $I_D$, as shown in Fig. 1(a). The period of oscillation $T_{\text{Conv}}$ is given by

$$T_{\text{Conv}} = C(V_H - V_L)/I_C + C(V_H - V_L)/I_D + 2t_{\text{delay}}$$

where $V_H$ and $V_L$ are the two preset bang-bang voltages, and $t_{\text{delay}}$ is the delay time from the comparator inputs to the Set/Reset (SR)-latch outputs. Delay time $t_{\text{delay}}$ can be designed to be as short as the hold time required by the SR inputs. Now, on-chip capacitors have relatively small TC, and $t_{\text{delay}}$ is negligibly short; therefore, the TC of the output frequency is mainly due to the TCs of $I_C$ and $I_D$. Unlike a bandgap voltage reference that has ultralow TC, $I_C$ and $I_D$ are very difficult to be designed to have low TCs. As a result, the conventional relaxation oscillator is not suitable to serve as a frequency reference.

B. PDRO

To eliminate the current terms in (1), a pseudodifferential relaxation oscillator (PDRO) is employed, as shown in Fig. 1(b). Two matched currents $I_1 = I_2$ are set to go through a composite resistor and two time-interleaved capacitors $C_1$ and $C_2$. In this topology, reference voltage $V_R$ is generated by $I_1 \times R$, and while $C_1(C_2)$ is charged up by $I_2$, $C_2(C_1)$ is discharged by a small switch $S_4(S_3)$. In this design, $I_1$ and $I_2$ are 500 nA, and for switches $S_1$ and $S_2$, the size needed is only 2 μm/0.35 μm. When voltage $V_C$ is charged up to $V_R$, the comparator outputs a “High” and triggers the D flip-flop (DFF) that serves as a frequency divider. In the next clock phase, $C_1$ and $C_2$ are swapped by $S_1$ and $S_2$, and $V_C$ drops to 0 and is charged up again. Consequently, the comparator output goes back to 0, resulting in a short pulse that serves as the clock signal for the DFF. The pulse width is the delay time $t_{\text{delay}}$ of the comparator-DFF-switch loop, which only needs to be larger than the hold time of the DFF clock input. The main concern of minimizing $t_{\text{delay}}$ is the power consumed by the comparator and switches that are scalable with process.

Benefiting from the interleaving topology, discharging switches $S_3$ and $S_4$ can be small as they have half a cycle to discharge $C_1$ and $C_2$. To avoid charge sharing between $C_1$ and $C_2$, $S_1$ and $S_2$ should not be turned on simultaneously. In other words, the DFF outputs, i.e., $Q$ and $ar{Q}$, should have a nonoverlapping characteristic, and this is realized by asymmetrical pMOS and nMOS ratios for the DFF output inverters. The period of the PDRO $T_{\text{PDRO}}$ is given by

$$T_{\text{PDRO}} = \frac{C_1V_R}{I_0} + \frac{C_2V_R}{I_2} + 2t_{\text{delay}} = \frac{I_1}{I_2}(C_1 + C_2)R + 2t_{\text{delay}}.$$  \hspace{1cm} (2)

Currents $I_1$ and $I_2$ are designed to be well matched, that is, $I_1 = I_2$, and

$$T_{\text{PDRO}} = (C_1 + C_2)R + 2t_{\text{delay}} \approx (C_1 + C_2)R.$$  \hspace{1cm} (3)

The mismatch between $C_1$ and $C_2$ only affects the duty ratio of the output frequency; hence, the matching requirement is not demanding. The capacitor $C_3$ that is in parallel with the composite resistor is used to filter the noise on the $V_R$ node. Ideally, the switching period would only be determined by the on-chip passive components.

C. Composite Resistor With Proposed Switch Array

While the on-chip capacitor has a small TC of 30 ppm/K, all on-chip resistors have nonideal temperature characteristics, as listed in Table II (in a 0.35-μm 2P4M CMOS process), that are characterized by the foundry. To obtain a low-TC resistor, both +TC and −TC resistors (HR-Poly and R-Poly2 in this case) have to be used for TC cancelation. However, the accuracy of the simulation model is only guaranteed by using the suggested dimension that is usually area consuming [10]. For example, the models of resistors in this process are characterized with a width larger than 4 μm. Other error sources, such as contact resistor $R_{\text{E}}$, comparator input offset voltage, delay time, and...
TABLE II
TC OF THE ON-CHIP COMPONENTS

<table>
<thead>
<tr>
<th>On-Chip Component</th>
<th>Sheet R (Ω/μm²)</th>
<th>1st-Order TC (10⁻⁵/K)</th>
<th>2nd-Order TC (10⁻⁶/K²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HR-Poly</td>
<td>1.2k</td>
<td>-0.75</td>
<td>3.82</td>
</tr>
<tr>
<td>R-Poly1</td>
<td>8</td>
<td>0.9</td>
<td>N/A</td>
</tr>
<tr>
<td>R-Poly2</td>
<td>50</td>
<td>0.59</td>
<td>0.77</td>
</tr>
<tr>
<td>R-NWell</td>
<td>1k</td>
<td>6.2</td>
<td>N/A</td>
</tr>
<tr>
<td>C-Poly</td>
<td>N/A</td>
<td>0.03</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Fig. 2. Composite resistor for low-TC trimming with (a) PRA and (b) the proposed PSA.

current mirror mismatch, would also add inaccuracy to the output frequency. Furthermore, even if the first-order TC could be well compensated, the second-order TC coefficients of HR-Poly and R-Poly2 will considerably affect TC cancelation over a wide temperature range.

The method of programmable resistor array (PRA) is a common practice for resistor value trimming, as shown in Fig. 2(a). However, there is a tradeoff between on-resistance $R_{ON}$ and leakage current when sizing the switches. In high-precision trimming, the PRA method has several drawbacks. First, to bypass small resistors, large switches with much smaller on-resistance are needed that result in considerable leakage current from the transistor gates and/or parasitic pn junctions. Second, resistor segments suffer from parasitic contact resistor $R_{End}$ that varies by as much as ±50% over process and has a much larger TC (thousands of parts per million per degree Kelvin). Third, the multiple-switch on-resistors in series with the trimming resistors would affect the TC cancelation accuracy. Thus, TC trimming with PRA is hardly well controlled.

Instead of using switches to bypass small resistors, the intrinsic $R_{ON}$ of the switches is employed to trim the TC in this proposed PSA, as depicted in Fig. 2(b). The sizes of switches in PSA are much smaller than those in PRA, as $R_{ON}$ does not need to be that small. As a result, gate leakage is much reduced. The switch $R_{ON}$ is given by

$$R_{ON} = \frac{1}{\mu_n C_{ox} (W/L)_{SW} (V_G - V_{TH})}. \quad (4)$$

To eliminate $R_{ON}$ variation with gate voltage $V_G$, a simple voltage regulator that only consumes 0.4 μA is used to set $V_G$ of the switch array, as shown in Fig. 3(a). As $V_G$ is generated by a diode-connected MOS field-effect transistor with a drain current of $I_B/2$, (4) can be expressed as

$$R_{ON} = \frac{1}{\sqrt{I_B \mu_n C_{ox} (W/L)_{SW}^2/(W/L)_B}}. \quad (5)$$

Accuracy can be further improved by using more bits for trimming, as even a large switch array has a very small area overhead and a system-on-chip can accommodate many control bits. The simulated temperature curve of $R_{ON}$ of the D⟨3⟩ switch with a constant drain current is plotted in Fig. 3(b).
The first- and second-order TC terms of $R_{ON}$ extracted by the MATLAB “polyfit” function are $2.18 \times 10^{-3}/K$ and $-3.84 \times 10^{-6}/K^2$, respectively. While both second-order TCs of HR-Poly and R-poly2 are positive, the second-order TC of $R_{ON}$ is negative, helping in overall TC compensation.

To minimize current consumption, the resistance in the relaxation oscillator is in the submegaohm range. From (5), $R_{ON}$ is in the 10-kΩ range if $I_B$ is in the submicroampere range. Let the ratio of $R_{+TC}$ to $R_{ON}$ be $\alpha$; then, to obtain a zero-TC composite resistor with three resistor types, the condition to be satisfied is

$$\left(T - T_0\right)(T^{SW}R_{ON} + TC^+R_{+TC} + TC^-R_{-TC}) = 0$$  \hspace{1cm} (6)

$$\left(T^{SW}R_{+TC}/\alpha + TC^+R_{+TC} + TC^-R_{-TC}\right) = 0.$$  \hspace{1cm} (7)

By combining the two +TC components, we have

$$\frac{R_{+TC}}{R_{TC}} = \frac{-TC^-}{TC^+ + T^{SW}/\alpha}.$$  \hspace{1cm} (8)

D. Bias Circuit and Startup Circuit

A self-biased circuit operating in the subthreshold region is used to generate the bias current $I_B$ that is given by

$$I_B = \ln N \times V_T/R_B = \ln 2 \times V_T/R_B$$  \hspace{1cm} (9)

where $N$ is the ratio of $M_2$ and $M_1$. Here, $N$ is set to be 2 to get a smaller $I_B$ with the same resistance of $R_B$. Cascode current mirror is used to increase the $V_{DD}$ immunity and to get better matching between $I_B$, $I_1$, and $I_2$.

Quiescent current of the startup circuit is eliminated by using a system-controlled pulse to jump start the bias circuit, as shown in Fig. 4. When the “St-up” pin is pulled high by a one-shot pulse, $V_A$ will be pulled high, activating $M_7$ and $M_6$ through $M_1$, and the local negative feedback loop of $M_6$ and $M_7$ prevents a large current to flow from $M_6$ to $M_1$. When “St-up” is restored to “High,” $M_6$ and $M_7$ are cut off, and the startup circuit now consumes no current and is isolated from the bias circuit.

E. Comparator Design

The first two stages of the comparator are biased with unequal currents, as shown in Fig. 5, with 1.6 μA for the first stage and only 100 nA for the second stage, because the comparator only needs to have fast rising-edge to trigger the DFF clock input when comparing $V_C$ and $V_R$. The size of $M_7$ is much larger than that of $M_5$ and $M_6$ to increase its pull-down capability. In addition, $M_3$ has a relatively large size to pull up the output faster. After $C_1$ and $C_2$ are swapped (see Fig. 1), the comparator output will flip to low gradually. Although the comparator consumes most of the current of the relaxation oscillator, smaller power consumption could be achieved in a more advanced process.

III. Measurement Results

The prototype chip, shown in Fig. 6, was fabricated in a 0.35-μm CMOS process with an area of 0.162 mm². The resistor width was conservatively chosen to be 4 μm as recommended in the process document. Hence, most of the area is occupied by resistors. The PSA uses 8-bit trimming. Three samples from the same batch were characterized, and the trimmed temperature stability was measured to be ±0.5% from $-20$ ℃ to 100 ℃ at $V_{DD} = 1.5$ V, as shown in Fig. 7. From simulation, the default code for the smallest TC is “0000 1000”; whereas from measurement, the code for sample 1 was “0100 0000” and that for samples 2 and 3 was “0001 0000.” The output frequency change was within ±0.4% as the supply voltage changed from 1.0 to 3 V, as reported in Fig. 8. The histogram of 156 k clock cycles from one prototype chip is shown in Fig. 9. The standard deviation of frequency $\sigma_f$ is 87.3 Hz (0.07% of 132 kHz). Resistance ratios good for mass production have not been established as only one batch of oscillators has been fabricated and measured. For the absolute accuracy, it can be trimmed by a capacitor array that has comparatively negligible
IV. CONCLUSION

In this brief, pseudodifferential architecture with two interleaved charging/discharging capacitors has been employed in the design of the relaxation oscillator, and a novel TC trimming scheme that uses switch $R_{ON}$ in series with the composite resistor achieving first- and second-order TC compensation has been proposed. Based on measurements over the whole temperature range, the prototypes were trimmed with good temperature stability. It should be noted that using the proposed PSA, initial TC accuracy of the composite resistor is no longer a problem. Thus, the resistor width could be dramatically reduced and so does the silicon cost. If the resistor width is changed from 4 to 1 $\mu$m, the resistor area will shrink to only 10% of the current value, and over 50% area reduction of the whole oscillator could be achieved. Therefore, the proposed design is suitable for low-voltage low-cost one-chip systems such as crystal-less radios or wireless sensor nodes.

REFERENCES


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