Analysis and Design of an Ultrabroadband Stacked Power Amplifier in CMOS Technology

Hai-Feng Wu, Student Member, IEEE, Qian-Fu Cheng, Student Member, IEEE, Xu-Guang Li, and Hai-Peng Fu, Member, IEEE

Abstract—This brief presents the analysis and design of a two-stage stacked power amplifier (PA) with very broadband gain frequency response and power performance in a small chip size. The broadband load impedance match is realized using modified stacked field-effect transistors (FETs) with a resistive feedback by analyzing the matching condition of the source input impedance of the stacked FET. In order to further improve the broadband gain frequency response, the effectiveness of a gain expansion from a stacked driver amplifier is demonstrated to compensate the gain compression of the last-stage amplifier. To verify the design concept, a two-stage three-stacked PA has been implemented in a 0.18-$\mu$m CMOS technology. The PA achieves a saturated output power of 22–24.3 dBm and a power added efficiency of 13%–20% within a 194% fractional bandwidth from 0.1 to 6.5 GHz. It also demonstrates better than 11-dB input return loss (RL) and better than 5.1-dB output RL. This PA occupies a chip size of 0.64 mm$^2$ including pads.

Index Terms—Broadband power amplifier (PA), CMOS PA, resistive feedback, stacked amplifier, stacked PA.

I. INTRODUCTION

DURING recent decades, modern wireless communication/broadcasting systems have experienced a remarkable development and growth, with an increasing number of standards in the VHF/UHF/L/S/C bands, such as RFID, GSM, DAB, GPS, DVB-H, Bluetooth, WLAN, etc. [1]–[4]. Growing together with the proliferation of these standards, there is a demand for the integration of multiple standards into a single portable terminal [5]. To fulfill this demand, the software-defined radio (SDR) combined with the modern CMOS technology offers a powerful platform. The SDR can be used across different frequency bands and for multistandard applications [6], and the CMOS technology has the potential to integrate the radio frequency (RF), analog, and digital parts into a single system-on-chip radio [7]. However, some SDR systems need to be equipped with really broadband RF frontends to properly exploit the reconfiguration possibilities provided by the digital section [8]. Accordingly, as critical components in the RF frontends, the power amplifiers (PAs) need to maintain a broadband response when implemented for these SDR systems. Thus, it is attractive to realize a broadband PA using CMOS technology in the previously mentioned VHF/UHF/L/S/C bands.

The main challenge to design a broadband PA is to maintain wideband gain frequency response and broadband power performance simultaneously [9]. Especially in the CMOS process, it is challenging to achieve a broadband PA for output powers beyond 100 mW owing to the limitations of the low breakdown voltage and the high impedance transformation ratio (ITR) across the operating frequency range [10], [11]. Moreover, due to thin metal layers and conductive Si substrate, on-chip inductors and transformers suffer from low quality factor, which makes on-chip matching networks extremely lossy and narrow-band [12]. Considering these problems, several methods have been proposed to achieve the CMOS PA's broadband performance. As a traditional method, a travelling wave amplifier demonstrates multioctave bandwidth (BW) result. However, it has a relatively low efficiency or a large chip area [13], [14]. Similarly, if the ITR is high, designing wideband matching circuits suffers from having a large dimension, as well as high RF loss, which severely degrades the amplifier output power and efficiency [15].

The transistor-stacking technique is theoretically possible to solve the aforementioned problems. By connecting several transistors in series, the stacked transistors obtain a multiple higher output voltage swing to overcome the low breakdown voltage for high output power. Meanwhile, the optimum load impedance becomes higher as the number of stacked transistors increases, resulting in reduced ITR to allow a broadband behavior [17], [18]. Moreover, its high optimum load impedance is possible to be matched to 50 $\Omega$ without using any on-chip matching network, which simplifies the circuitry and reduces the chip area [11], [17]. Due to these merits, various stacked PAs have been proposed to improve the efficiency, the BW, and the output power [16]–[22]. Most of these PAs were typically based on an analysis of the source input impedance (SII) of the stacked transistors. However, the conventional method to calculate the SII must be corrected to account for pronounced effects of the gate–drain capacitance ($C_{gdl}$) in Si MOSFETs [23].

This brief presents the analysis and design of an ultrabroadband PA using two-stage three-stacked field-effect transistors (FETs) in a 0.18-$\mu$m CMOS technology. Considering the effects of $C_{gdl}$ in the stacked FET, a corrected equation to calculate the SII is implemented to design a modified stacked amplifier. Due to the gain compensation from the driver amplifier to the last-stage amplifier, this two-stage PA achieves larger than 22 dBm (158 mW) output powers in 0.1–6.5 GHz. In contrast to most other reported CMOS PAs, the proposed PA occupies a small chip size and maintains a good merit on...
the combination of gain flatness, output power, power added efficiency (PAE), BW, and input/output matching.

This brief is organized as follows. Section II reviews the transistor-stacking technique and the SII of the stacked FET. Section III introduces the topology of a modified three-stacked amplifier. Based on this topology, a broadband two-stage three-stacked PA is presented in Section IV. Section V shows the measurement results, and Section VI provides the conclusion.

II. ANALYSIS OF TRANSISTOR-STACKING TECHNIQUE

As the technology scales down, the high-power broadband CMOS PA design becomes more difficult due to the low breakdown voltage and the low output impedance. Limited by the maximum allowable voltage, many large devices have been typically connected in parallel to increase the current swing for a high output power. However, the paralleled devices have a lower output impedance, which require to be matched to 50 Ω with a high ITR. More seriously, the high ITR increases the loss contribution of the mismatching network and significantly reduces the matching BW [24]. Thus, one possible strategy to maintain a broadband power performance is to combine low operating voltages and synthesize low output impedances close to 50 Ω. The transistor-stacking technique is such an attractive solution.

A. Typical Transistor-Stacking Configuration

Various configurations based on the transistor-stacking technique have been proposed to achieve the voltage combining. Among them, the HiVP FET is a typical n-stacked FET (n = 3) as illustrated in Fig. 1. Ideally, each FET (M1 - M3) in this circuit has the same drain–source, gate–source, and gate–drain voltage swings. Since these devices are connected in series and their drain–source voltages combine in phase, the total voltage swing of the n-stacked FETs is n times higher than the drain–source voltage swing of the single FET (Vds) accordingly. Meanwhile, the total current swing (Im) remains constant. As a result, the output power and the output impedance of the n-stacked FETs are n times higher than the single FET. More importantly, the optimum load impedance of the n-stacked FETs (n · Zopt) can be synthesized close to the standard 50-Ω load, which simplifies the output matching network and allows a broadband behavior. In this way, the stacked FETs can possibly improve the broadband power performance of the CMOS PA.

Besides the stacked transistors, the resistors R1 - R3 are used to provide gate biasing. Moreover, R3 works as a feedback resistor to allow maximum voltage swing. Due to this resistor, each gate voltage of the stacked FETs swings together with the drain voltage of the top FET (M3), which avoids the early gate–source breakdown [19]. Two inductors Lg and Ld serve as RF chocks to feed dc power to the gate and drain, respectively.

Fig. 1. Schematic of the n-stacked FETs (the HiVP configuration).

The main difference between the conventional cascoding devices and the stacked FETs is the voltage swing at the gate of the transistor. The gate of the common-gate (CG) transistor in the conventional cascading device is RF-grounded, which makes the gate–drain voltage swing of the CG transistor become a bottleneck [25]. In contrast, the external capacitances (C1 and C2) are introduced to allow RF swings at the gates of the stacked FETs. The external capacitances and the gate–source capacitances (Cgs) of the stacked FETs are used as a capacitive voltage divider to produce the proper in-phase voltage swings at the gates and drains, which systematically reduces the gate–drain and drain–source voltage swings of both the common-source and CG transistors under large signal condition [20]. Thus, the stacked FETs allow a more reliable transistor operation for high output power.

More importantly, the external capacitances (C1 and C2) are also useful in achieving the internal impedance matching among the stacked FETs. They can adjust the optimum load impedance (Zlk) seen at the drains of the middle and bottom FETs (M1 and M2), as in Fig. 1. The kth FET’s SII (Zsk) is the (k − 1)th FET’s load impedance (Zlk(k−1)). Thus, Zsk should be set to (k − 1) · Zopt by adjusting the external capacitances Ck. When neglecting the parasitic capacitances, here the optimum load impedance Zopt of a single FET is

\[ Z_{opt} = \frac{V_m}{I_m} \approx \frac{V_{ds} - V_{knee}}{I_{ds}} \quad (1) \]

where Vds and Ids are the drain–source voltage and current, respectively, and Vknee is the knee voltage. It is noteworthy that (1) is suitable for a linear amplifier for \( f_0 \ll F_s \), as in [10] and [17]. When some protocols prefer the nonlinear PAs for high efficiencies, the linear PA design may not be suitable. However, the nonlinear PA is a conventional narrowband. Thus, multiband PAs which maintain high PAEs over multiple narrowband frequency bands are attractive for these protocols in certain SDR systems. Therefore, a general wideband PA is not the unique choice.

The aforementioned analysis shows the basic theory of the n-stacked FETs for achieving high-power broadband performance.

B. Optimum Load Impedance of a Stacked Amplifier

An equivalent circuit model of the kth stacked FET is shown in Fig. 2, which is composed of \( C_k, C_{gds}, C_{gds}, Z_{lk}, g_{m}, \) the transconductance \( g_{m}, \) the gate–source conductance \( g_{ds}, \) and the drain–source capacitance \( C_{ds}. \) Based on this circuit, the SII of the kth stacked FET (Zsk) is expressed as follows (k > 1):

\[ Z_{sk} = R_{sk} + jX_{sk} = \frac{(m + j\omega n)}{(p + j\omega q)} \quad (2) \]

Fig. 2. Effect of an external gate capacitance on a stacked FET’s SII.
where

\[ m = (C_{gd} + C_{gs} + C_k)(1 + G_{ds}Z_{Lk}) + Z_{Lk}C_{gd}g_m \]

\[ n = Z_{Lk}C_{gd}(C_{gs} + C_k) \]

\[ p = G_{ds}(C_{gd} + C_{gs} + C_k) + g_m(C_{gd} + C_k) - \omega^2 Z_{Lk}C_{gd}C_{gs}C_k \]

\[ q = C_{gs}(C_{gd} + C_k) + G_{ds}Z_{Lk}C_k(C_{gd} + C_{gs}) + Z_{Lk}C_{gd}C_kg_m. \]

This equation was verified using MATLAB and ADS simulation. After ignoring \( C_{gd} \) and \( G_{ds} \), (2) can be simplified to (3), which is the traditional expression in [19] and [20]

\[ Z_{sk} = \frac{(C_{gs} + C_k)}{(g_m + j\omega C_{gs})C_k} \approx \frac{(C_{gs} + C_k)}{g_m C_k} \text{ for } f_0 \ll f_t. \]

As illustrated in [23], relation (3) must be corrected to account for pronounced effects of \( C_{gd} \) in conventional Si MOSFETs. Considering \( C_{gd} \), (2) is a corrected relation to calculate \( Z_{sk} \). The differences between these two equations are illustrated in Fig. 3. By (2), the real part of \( Z_{sk} \) \( (R_{sk}) \) is closely correlated to the load impedance \( Z_{Lk} \), and different values of \( Z_{Lk} \) generate obviously different results of \( R_{sk} \) at the low frequency, which degrades a little at the high frequency. Meanwhile, the imaginary part of \( Z_{sk} \) \( (X_{sk}) \) with a small \( Z_{sk} \) degrades more than a large \( Z_{sk} \). However, by (3), \( Z_{sk} \) is uncorrelated to the load impedance \( Z_{Lk} \) when neglecting \( C_{gd} \). Thus, the effects of \( C_{gd} \) together with \( Z_{Lk} \) in conventional Si MOSFETs must be considered in stacked amplifier design. Moreover, a relatively steady frequency response of \( Z_{sk} \) can be obtained using the stacked structure over a quite BW as shown in Fig. 3. This is another reason why the stacked transistors are theoretically possible to allow a broadband behavior.

\[ Z_{sk} \text{ should be matched to } Z_{Lk}(k-1). \]

Based on (2), when neglecting \( X_{sk} \) and \( G_{ds} \), for \( f_0 \ll f_t, Z_{sk} \) can be matched near to \( Z_{Lk}(k-1) \), by adjusting the value of \( C_k \), as mentioned before. An approximate equation can be used to determine \( C_k \) as [21]

\[ C_k = \frac{(C_{gs} + C_{gd}(1 + g_m Z_{opt}))}{(k-1)g_m Z_{opt} - 1}, \quad k = 2, 3, \ldots, K. \]

III. STACKED-FET AMPLIFIER DESIGN

In order to design a broadband CMOS PA within a small chip size, a modified three-stacked amplifier is illustrated in Fig. 4(a). Unlike the traditional HiVP [19], the gate bias node of \( M_1 \) is directly connected to the ground through a resistor \( R_0 \). This self-biased structure simplifies the circuitry and reduces the chip size. To insure the identical biasing conditions of all FETs, the gate-biasing resistors \( (R_0 - R_3) \) are set as

\[ R_1 = R_2 = R_0 + R_3 = r_{ref} \]

\[ R_0 \]

\[ R_0 + R_3 = V_{gs} = V_{ds} = k \]

where \( k \) is the ratio of \( V_{gs} \) to \( V_{ds} \) and \( r_{ref} \) is a reference value.

A variety of mechanisms can lead to oscillatory behaviors of stacked-FET amplifiers. A well-known one is due to the capacitive loading of the source of the stacked transistor [23], which makes the amplifier potentially unstable. However, the dissipative combination of \( (R_0 - R_3) \) and the feedback resistor \( (R_f) \) stabilizes the stacked amplifier. In Fig. 4(b), a simulation shows their effects on the stability. Without \( R_f \), the amplifier is unstable when \( r_{ref} \) is \( 1e4 \) \( \Omega \) (line1). The stability is improved when \( r_{ref} \) is set to \( 500 \) \( \Omega \) (line1 versus line2), which makes the gate-bias network dissipative. As a result, a large \( r_{ref} \) will degrade the stability, while a small one will consume more dc power. A tradeoff can be obtained between these merits. Meanwhile, the stability frequency response is further improved by \( R_f \) at a high frequency (line3 versus line2). Fig. 5 shows simulations of the small signal gain \( (S_{21}) \) and stability factors \( (k_f \) and \( B1) \) versus \( R_f \). Although the stability degrades when \( R_f \) decreases, the BW of the gain frequency response is enlarged by suppressing the low-frequency gain. This can be used to design the driver amplifier to further enlarge the gain BW, as shown in Section IV.

IV. BROADBAND TWO-STAGE THREE-STACKED PA DESIGN

Based on the modified three-stacked amplifier, a two-stage PA is designed as shown in Fig. 6. The on-chip components are surrounded by the dashed line. The dc-blocking capacitances \( (C_1, C_2) \) and dc-feeding inductors \( (L_1, L_2) \) are off-chip. Both stages employ the structure illustrated in Section III. The last-stage amplifier is used to achieve the broadband power performance. Meanwhile, the driver-stage is used to obtain higher
frequency capability and gain BW than cascoding or common-source devices since \( n \)-stacked FETs can achieve a bonus gain of \( 10 \log_{10}(n) \) dB over the single FET [17]. Transistors \( M_1-M_6 \) are 800 \( \mu \)m/0.18 \( \mu \)m deep N-well NMOS to avoid the body effect, whose p-well bodies are connected to the source isolated from the substrate. All on-chip passive components share the same ground. \( C_2-C_7 \) are with values of 2.9, 5.9, 3, 2.9, 5.9, and 18 pF, respectively. Resistors \( R_3-R_6 \), as well as \( R_8-R_{11} \), are with values of 250, 500, 500, and 250 \( \Omega \), respectively. Resistors \( R_1 \) and \( R_{12} \) are with values of 20 and 6 \( \Omega \) to achieve ultrabroadband input matching of both stages, as in [15] and [17]. These are key factors in achieving a small chip size.

The last-stage amplifier is designed with \( R_7 \) of 370 \( \Omega \), generating a gain compression. The driver-stage amplifier is designed with \( R_2 \) of 70 \( \Omega \) to form a gain expansion versus frequency. As in Fig. 7, the gain compression of the last-stage amplifier is properly compensated by the gain expansion from the driver-stage amplifier. Thus, the BW of the broadband gain frequency response is further enlarged.

**V. MEASUREMENT RESULTS**

To verify the design concepts, a two-stage three-stacked PA was fabricated in a 0.18-\( \mu \)m CMOS process and measured on wafer, as shown in Fig. 8. This PA occupies a 0.64-mm\(^2\) chip size including pads. With 6-V supply voltages, the PA achieves a gain flatness of 18.4 \( \pm \) 1.5 dB, less than \(-11\) dB \( S_{11} \) and \(-5.1\) dB \( S_{22} \) in 0.1–6.5 GHz, as shown in Fig. 9. Comparing with the simulation, the measured \( S_{21} \) deteriorates due to the parasitic inductances of the dc probes when connecting to the ground. The difference of \( S_{22} \) curves is also mainly caused by these parasitics. This can be improved by bonding the decoupling capacitors to the ground pads when applied in a packaged chip.

Fig. 10 shows the measured saturated output power \( (P_{sat}) \) and PAE as a function of the frequency. From 0.1 to 6 GHz, the \( P_{sat} \) is above 22 dBm, and the PAE is above 17%. The \( P_{sat} \) is limited by the gate widths and the numbers of the stacked FETs. Thus, this design can be applied using more stacked devices with larger gate widths for a higher \( P_{sat} \), as in [20]. The feedback resistive networks of driver-stage and last-stage consume about 1.5% and 1.4% power, respectively. The three-stacked FETs of driver-stage and last-stage consume about 39.1% and 41% power, respectively. As one important specification in PA design, the AM–AM and AM–PM distortions at 3 GHz are...
plotted in Fig. 11. The PA demonstrates a gain variation of 0.5 dB as a function of the average output power ($P_{\text{ave}}$). Fig. 12 shows the measured ACLRs as a function of input power.

A second aspect of the linearity is the adjacent channel leakage ratios (ACLRs). Fig. 12 shows the measured ACLRs as a function of input power.

Table I lists the reported CMOS/BiCMOS PAs, and the comparisons with published broadband PA performances

<table>
<thead>
<tr>
<th>Ref.</th>
<th>CMOS Process</th>
<th>CMOS Freq.</th>
<th>Gain $S_1$</th>
<th>Gain $S_2$</th>
<th>$P_{\text{sat}}$</th>
<th>PAE (%)</th>
<th>Size (mm$^2$)</th>
<th>FoM $M_1$</th>
<th>FoM $M_2$</th>
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<tr>
<td>[3]</td>
<td>0.18-μm</td>
<td>2.6–5.4</td>
<td>15.8</td>
<td>&lt;&lt;5</td>
<td>11.5</td>
<td>0.16</td>
<td>9.4</td>
<td>2ε5</td>
<td></td>
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<tr>
<td>[4]</td>
<td>90-μm</td>
<td>5.2–13</td>
<td>18.5</td>
<td>&lt;&lt;10</td>
<td>22.6</td>
<td>0.70</td>
<td>4ε5</td>
<td>6ε6</td>
<td></td>
</tr>
<tr>
<td>[9]</td>
<td>0.18-μm</td>
<td>4–17</td>
<td>12/3</td>
<td>&lt;&lt;8</td>
<td>7.77</td>
<td>0.67</td>
<td>3ε4</td>
<td>7ε5</td>
<td></td>
</tr>
<tr>
<td>[12]</td>
<td>0.18-μm</td>
<td>3.7–8.8</td>
<td>8.24</td>
<td>&lt;&lt;8</td>
<td>12.6</td>
<td>2.8</td>
<td>3ε4</td>
<td>2ε5</td>
<td></td>
</tr>
<tr>
<td>[14]</td>
<td>BiCMOS</td>
<td>2–12</td>
<td>9.05</td>
<td>&lt;&lt;15</td>
<td>14.9</td>
<td>1.16</td>
<td>2ε5</td>
<td>5ε5</td>
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<tr>
<td>[16]</td>
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<td>0.68</td>
<td>2ε5</td>
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</table>

**This work**

0.18-μm 0.1–6.5 18.4 1.15 <<1 5.1 19–13–20 0.64 7ε5 6ε5

Max $P_{\text{sat}}$ PAE $S_2$ $S_1$ $S_2$ BW $f_c$

FoM$_1$ = $P_{\text{sat}}$ PAE $S_2$ $S_1$ $S_2$ BW $f_c$

FoM$_2$ = $P_{\text{sat}}$ PAE $S_1$ $f_c$ BW

(Based on the FoM introduced by ITRS)

Another aspect of the linearity is the adjacent channel leakage ratios (ACLRs). Fig. 12 shows the measured ACLRs as a function of input power.

Table I lists the reported CMOS/BiCMOS PAs, and the comparisons with published broadband PA performances.

VI. Conclusion

In this brief, a two-stage three-stacked PA has been analyzed and designed with broadband gain frequency response and power performance in a small chip size. A practical method has been developed to analyze the SII of the stacked FET. When implemented in a 0.18-μm CMOS process, this PA demonstrates a $P_{\text{sat}}$ larger than 22 dBm across 0.1–6.5 GHz within a chip size of 0.64 mm$^2$. This design concept also can be applied to achieve a higher output power if larger stacked devices were implemented. It is an efficient solution to design the low-cost high-power broadband CMOS PA for the SDR system.

Acknowledgment

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